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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K62

MLB

LAST_MODIFIED=

Tue Feb 8 15:20:30 2011

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REV

ECN

DESCRIPTION OF REVISION

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DATE

2011-02-08

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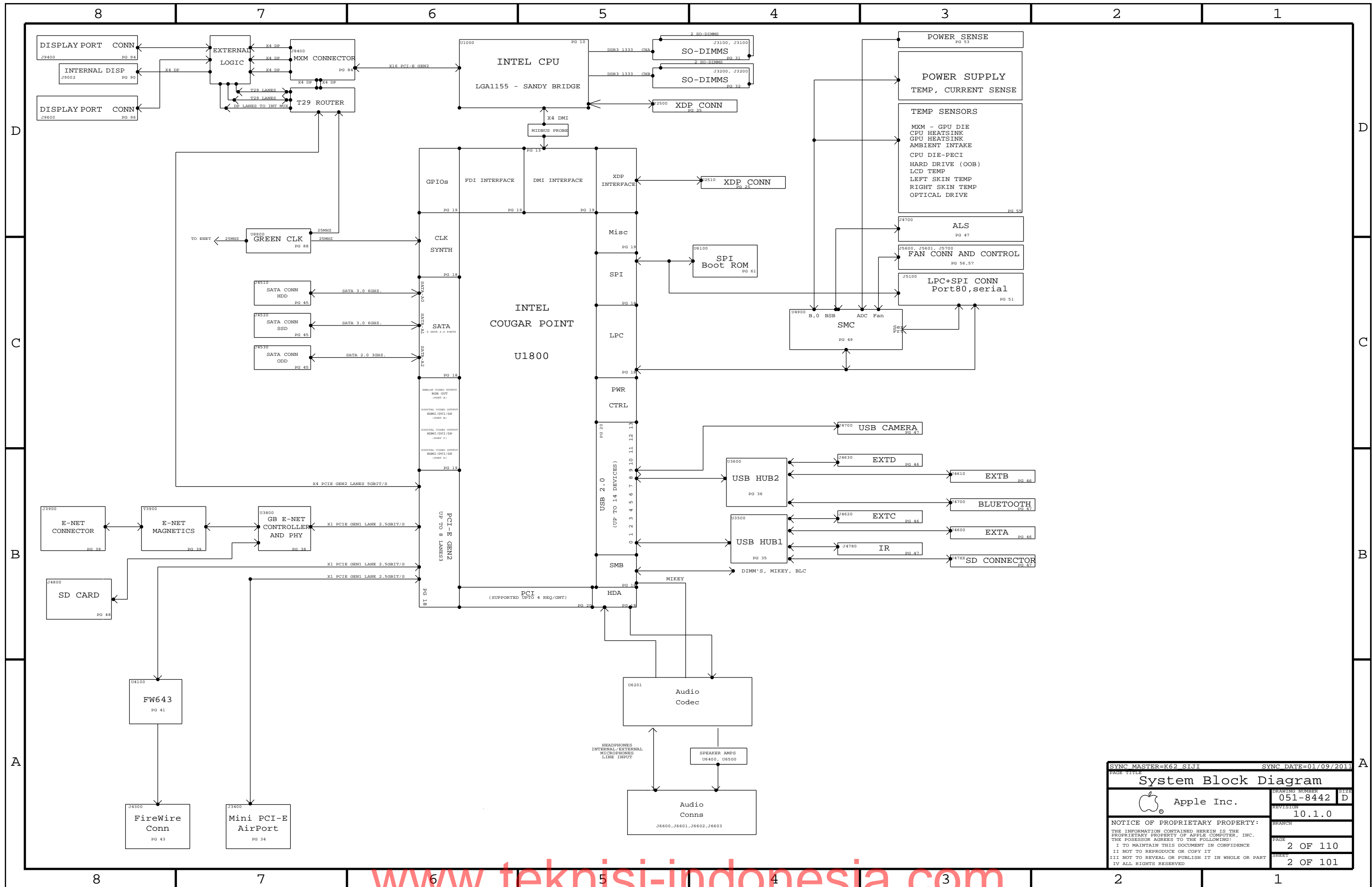
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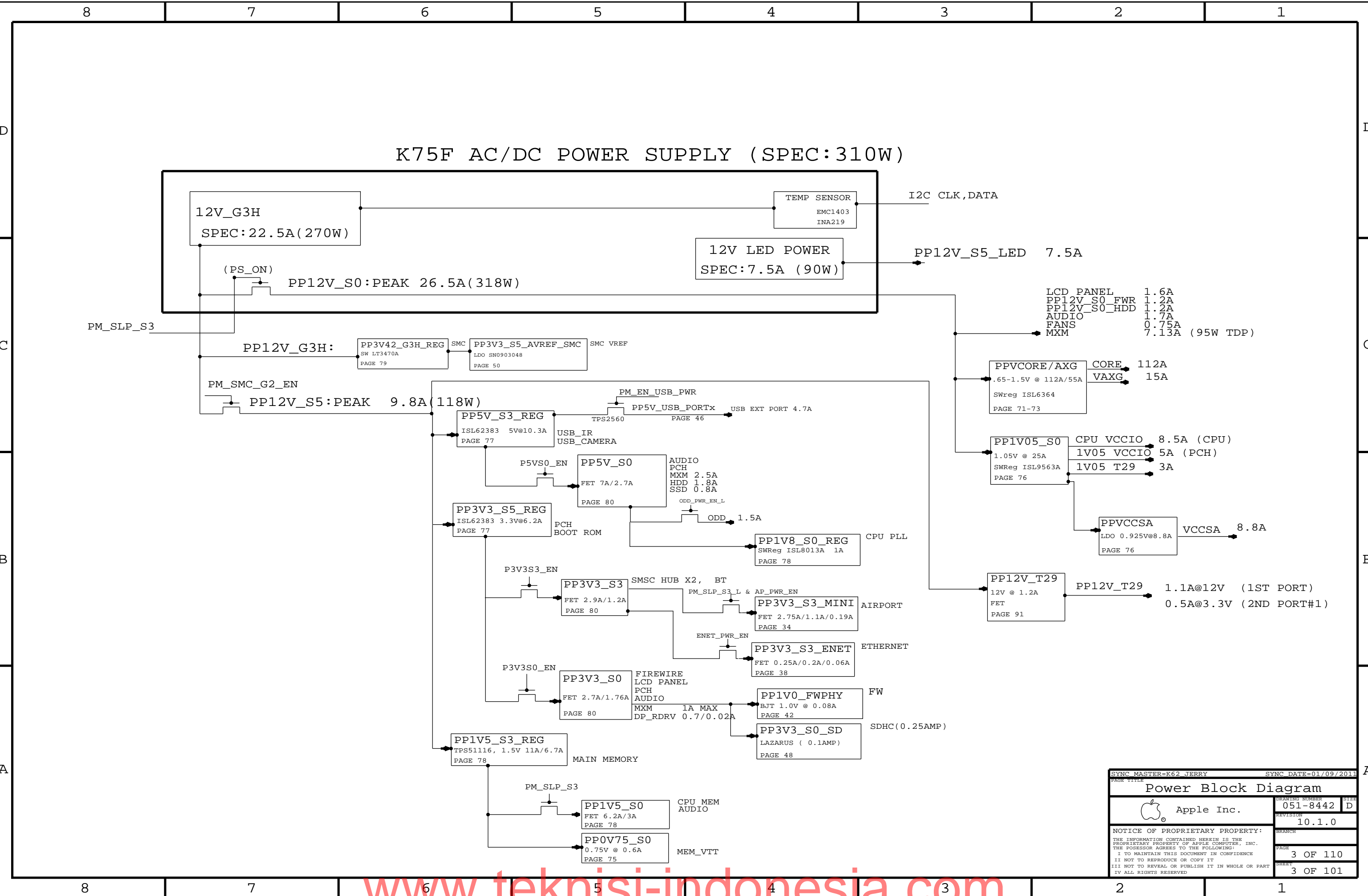
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| PAGE TITLE | | | |
| System Block Diagram | | | |
|  Apple Inc. | | DRAWING NUMBER | 051-8442 |
| | | REVISION | 10.1.0 |
| | | BRANCH | |
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D

C

B

A

BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|------------|--|---|
| 085-1226 | PCBA,MLB,DEV,K62 | DEVELOPMENT,DEV_GROUP |
| 639-1769 | PCBA,MLB,K62,2.8G,4C,PRQ,P2_ODD | K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG |
| 639-1770 | PCBA,MLB,K62,3.1G,4C,PRQ,P2_ODD | K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG |
| 639-1771 | PCBA,MLB,K62,3.4G,4C,PRQ,P2_ODD | K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG |
| 639-2186 | PCBA,MLB,K62,2.8G,4C,PRQ,P2_ODD,NO_DBG | K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG |
| 639-2187 | PCBA,MLB,K62,3.1G,4C,PRQ,P2_ODD,NO_DBG | K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG |
| 639-2188 | PCBA,MLB,K62,3.4G,4C,PRQ,P2_ODD,NO_DBG | K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG |
| 639-2124 | PCBA,MLB,K62,2.8G,4C,PRQ,P1_ODD | K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG |
| 639-2121 | PCBA,MLB,K62,3.1G,4C,PRQ,P1_ODD | K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG |
| 639-2123 | PCBA,MLB,K62,3.4G,4C,PRQ,P1_ODD | K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG |
| 639-2129 | PCBA,MLB,K62,2.8G,4C,PRQ,P1_ODD,NO_DBG | K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG |
| 639-2131 | PCBA,MLB,K62,3.1G,4C,PRQ,P1_ODD,NO_DBG | K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG |
| 639-2130 | PCBA,MLB,K62,3.4G,4C,PRQ,P1_ODD,NO_DBG | K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG |

BOM GROUPS

| BOM GROUP | BOM OPTIONS |
|-----------|--|
| BASIC1 | COMMON,ALTERNATE,MXM,FCIM,CPU_LV5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE |
| BASIC2 | HUB_USX2061,AP,BT,IR,T29,VAXG,PRODUCTION |
| DEV_GROUP | VREFMRGN_A,VREFMRGN_B,DIMM_LV5_SENSE |
| YES_DBG | XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES |
| NO_DBG | MOJOMUX:NO,LPCPLUS:NO |

CPU SOCKET & ILM SUB-BOMS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------|-------------------------|----------|--------------|
| 511S0071 | 1 | SOCKET,LGA1155,CPU-LF | U1000 | CRITICAL | TYCO_SOCKET |
| 604-1474 | 1 | ASSY,PURCHASED,ILM,TYCO | ILM | CRITICAL | TYCO_SOCKET |
| 511S0073 | 1 | SOCKET,LGA1155,CPU-LF | U1000 | CRITICAL | MOLEX_SOCKET |
| 604-1161 | 1 | ASSY,PURCHASED,ILM,MOLEX | ILM | CRITICAL | MOLEX_SOCKET |

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|------------|-------------------------------|--------------|
| 085-2451 | SUB ASSY,CPU SOCKET,K62,TYCO | TYCO_SOCKET |
| 085-2450 | SUB ASSY,CPU SOCKET,K62,MOLEX | MOLEX_SOCKET |

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-------------------------|-------------------------|----------|------------|
| 085-2451 | 1 | TYCO CPU SOCKET AND ILM | SKT_ILM | CRITICAL | |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|-----------------|
| 085-2450 | 085-2451 | | SKT_ILM | MOLEX ALTERNATE |

BOARD STACK-UP

| | |
|--------|--------|
| TOP | SIGNAL |
| 2 | GROUND |
| 3 | SIGNAL |
| 4 | POWER |
| 5 | POWER |
| 6 | SIGNAL |
| 7 | GROUND |
| BOTTOM | SIGNAL |

COMMON

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------------|-------------------------|----------|------------|
| 337S4088 | 1 | IC,CONJUG POINT,SLJ4F,BD82Z68,PRQ,B3 | U1800 | CRITICAL | |
| 353S3055 | 2 | IC,P13VEDP212,X2 DP MIX,QFN | U9390,U9590 | CRITICAL | |
| 338S0753 | 1 | IC,FW643,1394B_PCIE,PHY/LINK | U4100 | CRITICAL | |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | X14 | CRITICAL | |
| 343S0534 | 1 | IC,BCM57765,ENET&SD,8X8 | U3900 | CRITICAL | |
| 341T0184 | 1 | FLASH,EFI BOOTROM,K60/K62 | U6100 | CRITICAL | |
| 341T0328 | 1 | SFLASH ENET 2MBIT,CIV | U3990 | CRITICAL | |
| 338S0945 | 1 | T29 ROUTER, IC, ASSP | U9700 | CRITICAL | T29 |
| 341T0329 | 1 | IC,T29 SERIAL EEPROM | U9790 | CRITICAL | T29 |
| 341T0327 | 2 | IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25 | U9330,U9530 | CRITICAL | T29 |
| 341T0186 | 1 | IC,SMC,K62 | U4900 | CRITICAL | |

RAW: 335S0807

RAW: 335S0539

RAW: 335S0550

RAW: 337S3997

RAW: 338S0878

CPU5


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-------------------------------------|-------------------------|----------|----------------|
| 337S4042 | 1 | SNB,SR00D,PRQ,D2,2.8,95W,4+1,6M,LGA | CPU | CRITICAL | 2P8GHZ_SNB_CPU |
| 337S4040 | 1 | SNB,SR00Q,PRQ,D2,3.1,95W,4+1,6M,LGA | CPU | CRITICAL | 3P1GHZ_SNB_CPU |
| 337S4041 | 1 | SNB,SR00B,PRQ,D2,3.4,95W,4+1,8M,LGA | CPU | CRITICAL | 3P4GHZ_SNB_CPU |

K62 PARTS

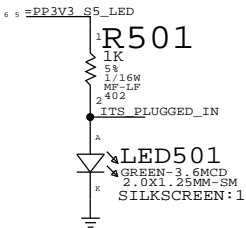
| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------|-------------------------|----------|------------|
| 051-8442 | 1 | SCH,MLB,K62 | SCH1 | | K62 |
| 820-2828 | 1 | PCBP,MLB,K62 | MLB1 | | K62 |

K62 ALTERNATE PARTS

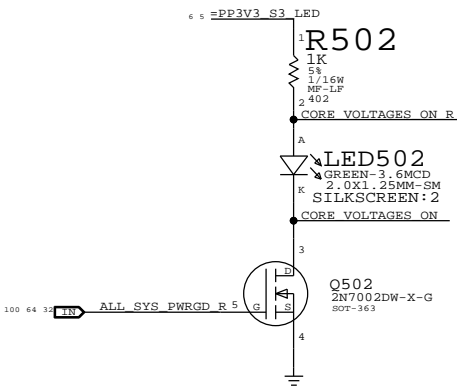
| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|--------------|
| 128S0298 | 128S0293 | | ALL | 330UF |
| 371S0679 | 371S0652 | | ALL | PIN DIODE |
| 377S0107 | 377S0066 | | ALL | USB DIODE |
| 376S0972 | 376S0612 | | ALL | ROHM TRA-BJT |

| | | | |
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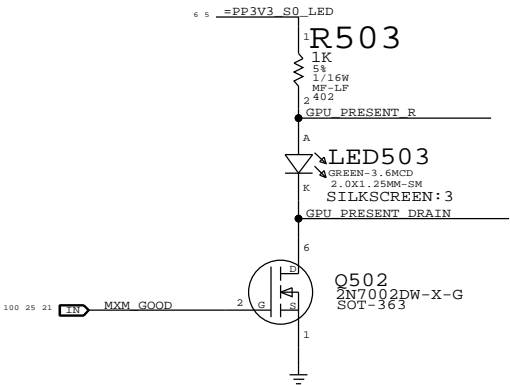
S5 Led



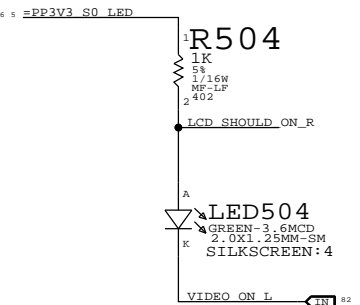
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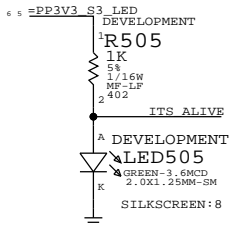
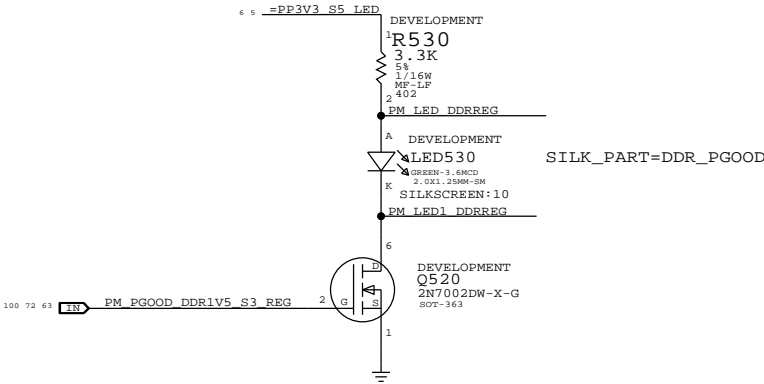
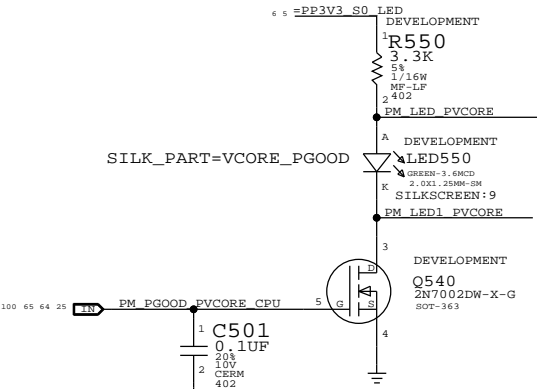
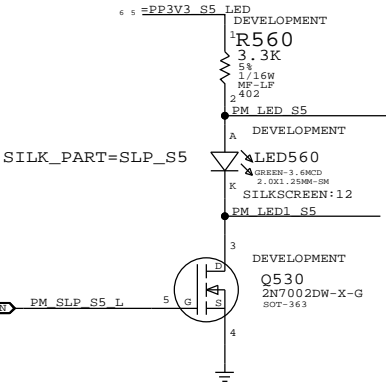
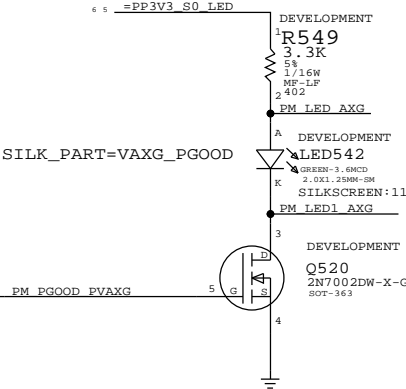
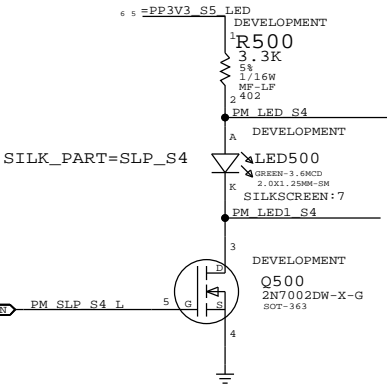
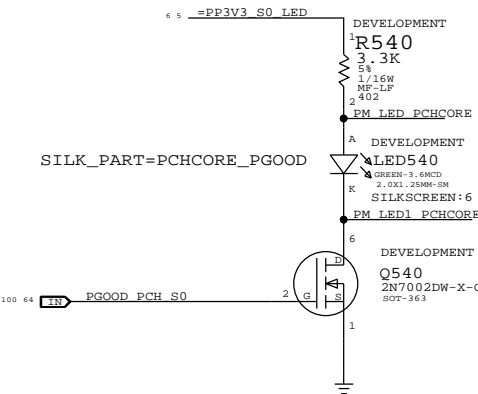
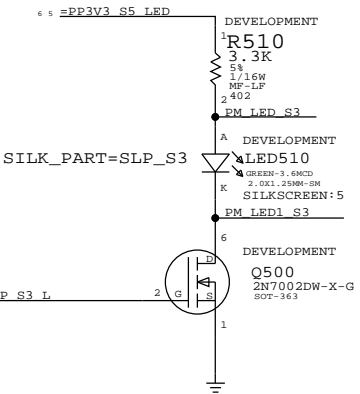
MXM PWR GOOD Led



VIDEO ON Led

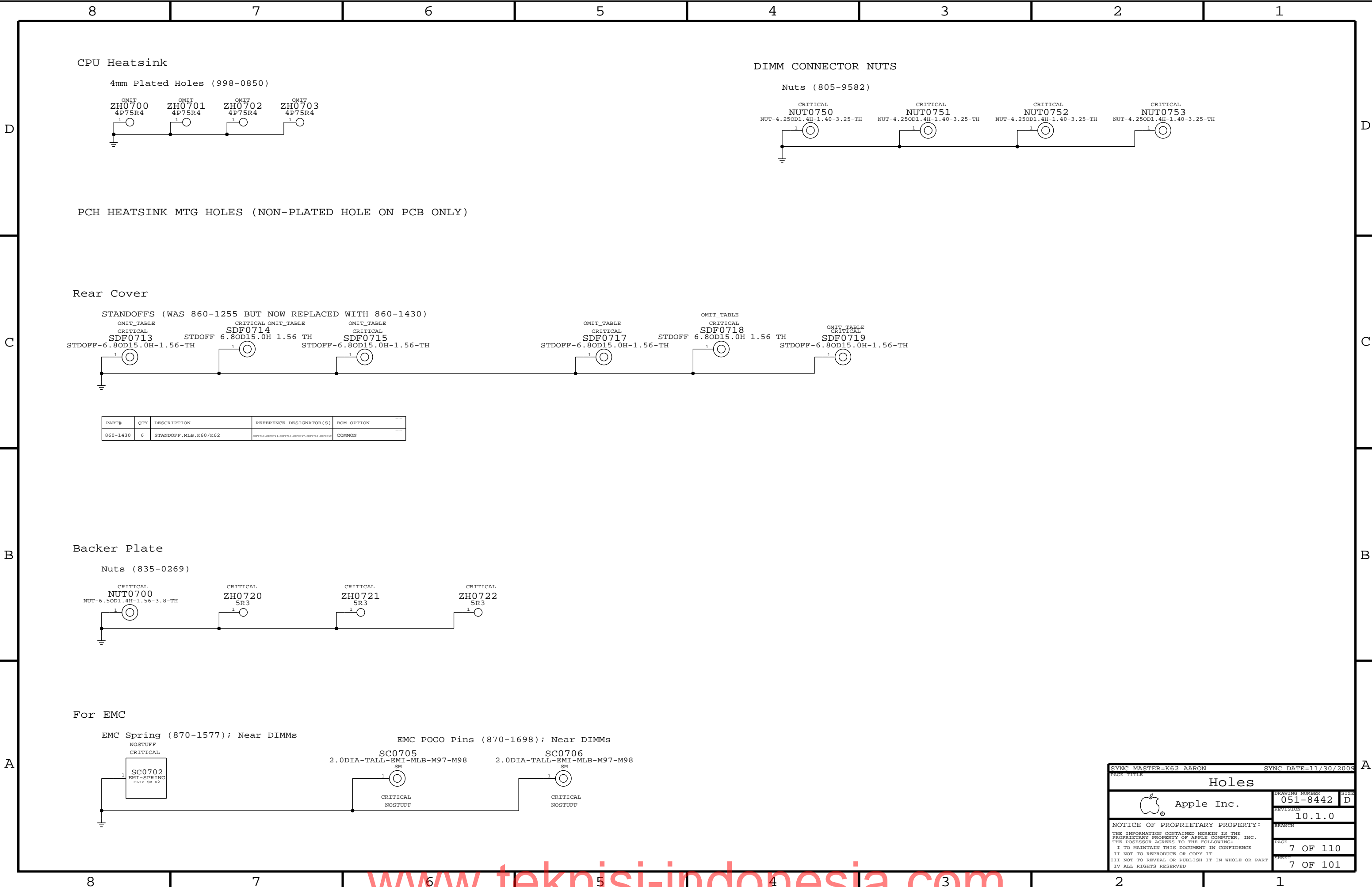


PROTO DEBUG LEDS ARE SHOWN BELOW



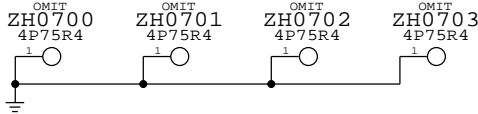
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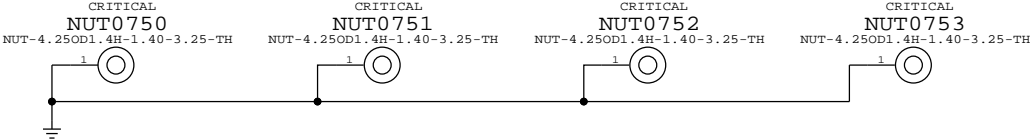
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK MTG HOLES (NON-PLATED HOLE ON PCB ONLY)

Rear Cover

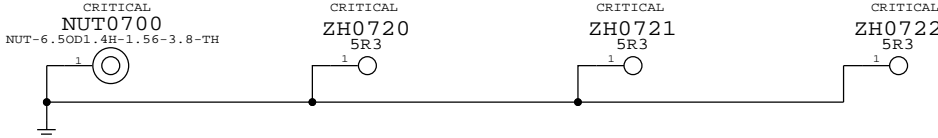
STANDOFFS (WAS 860-1255 BUT NOW REPLACED WITH 860-1430)



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|----------------------|---|------------|
| 860-1430 | 6 | STANDOFF,MLB,K60/K62 | SDF0713,SDF0714,SDF0715,SDF0717,SDF0718,SDF0719 | COMMON |

Backer Plate

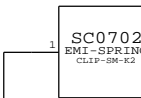
Nuts (835-0269)



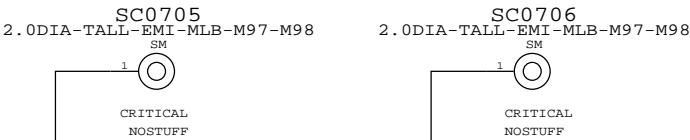
For EMC


EMC Spring (870-1577); Near DIMMs

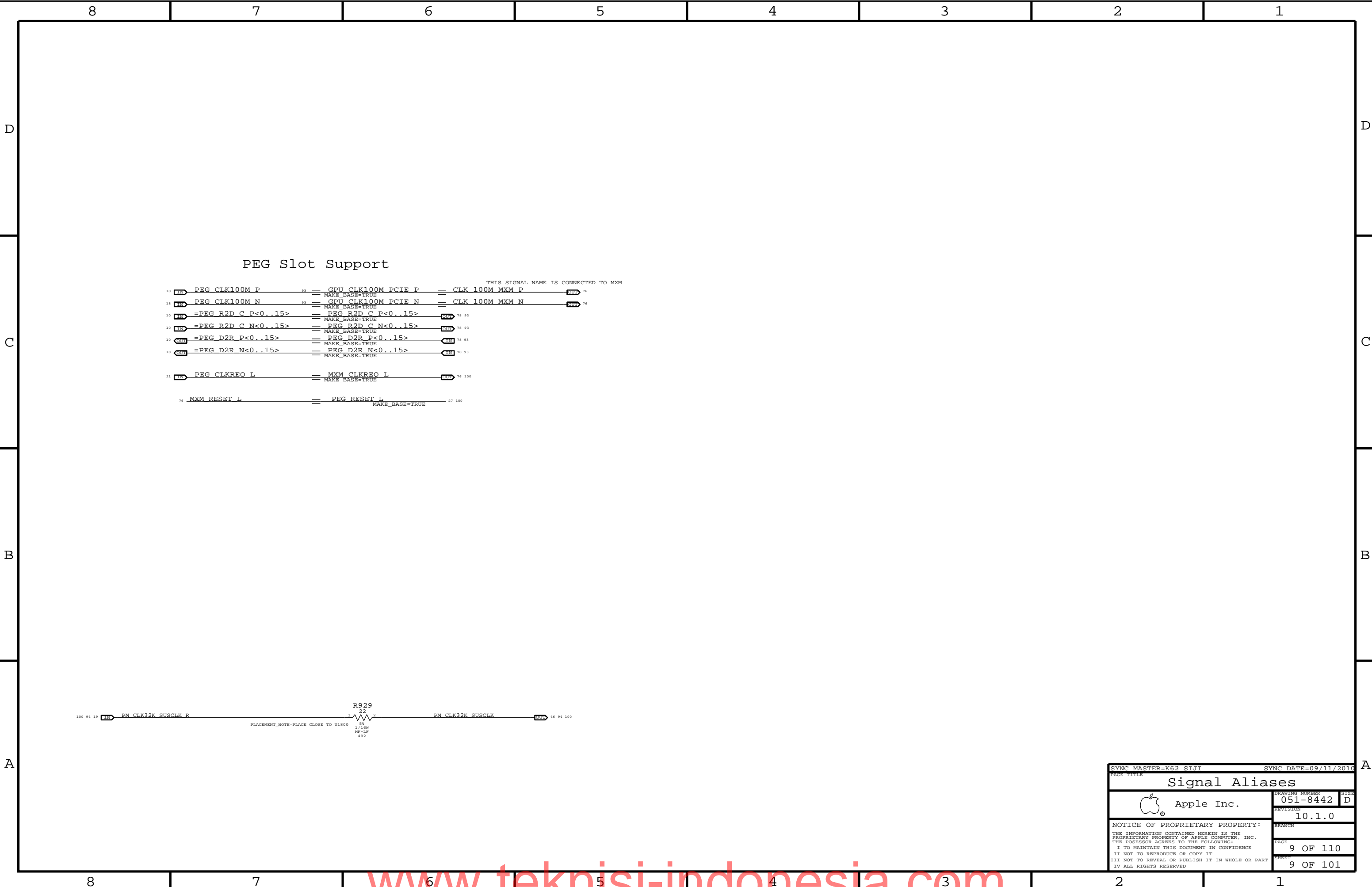
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CRITICAL

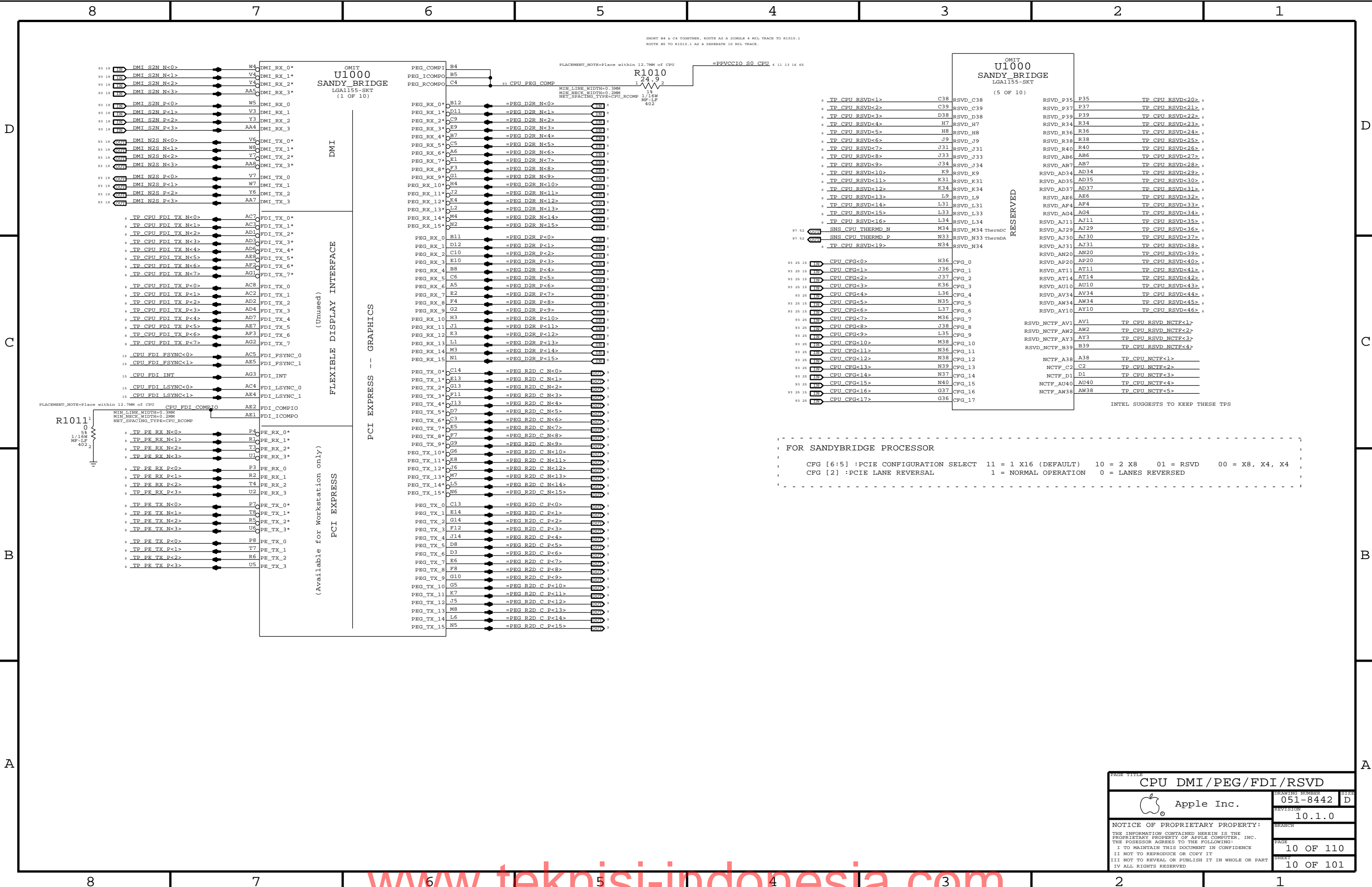



EMC POGO Pins (870-1698); Near DIMMs



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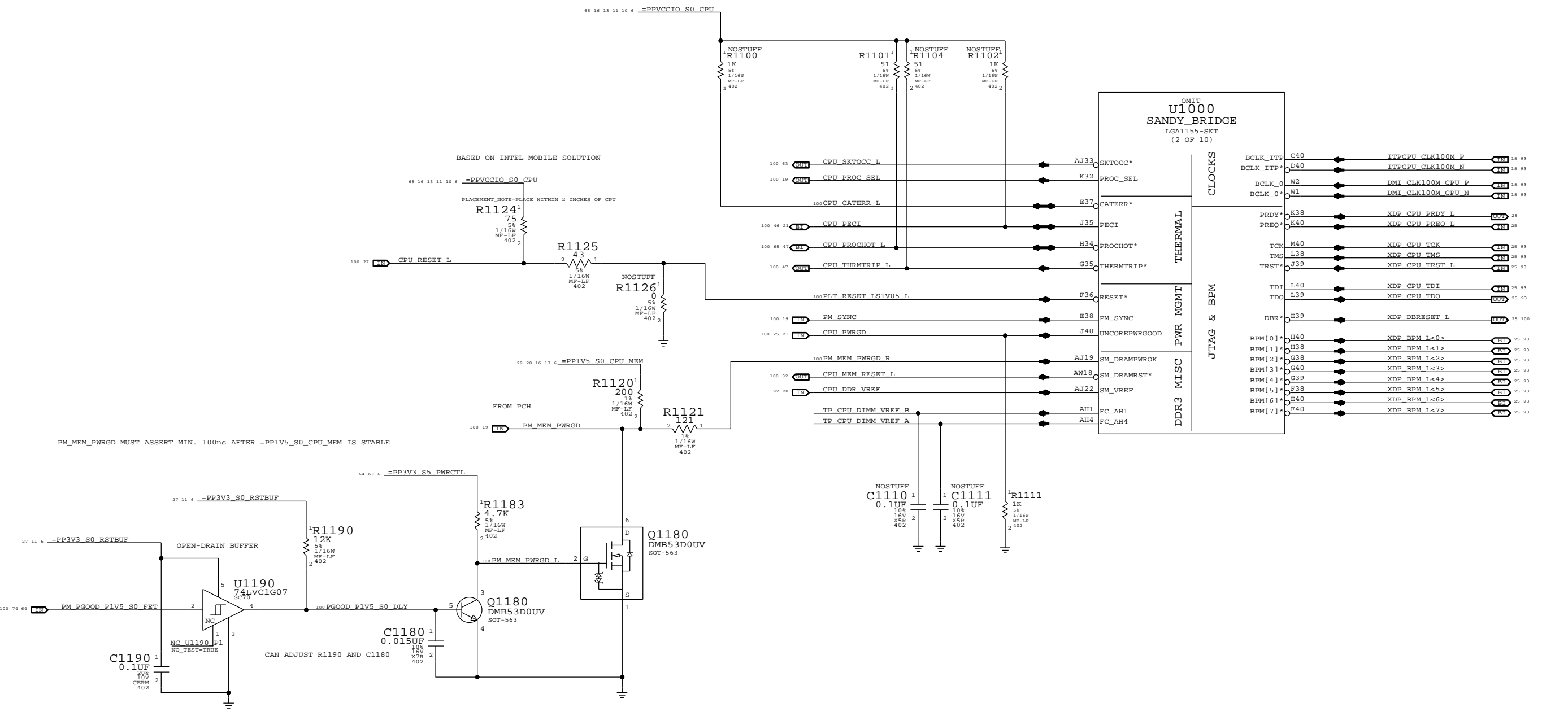
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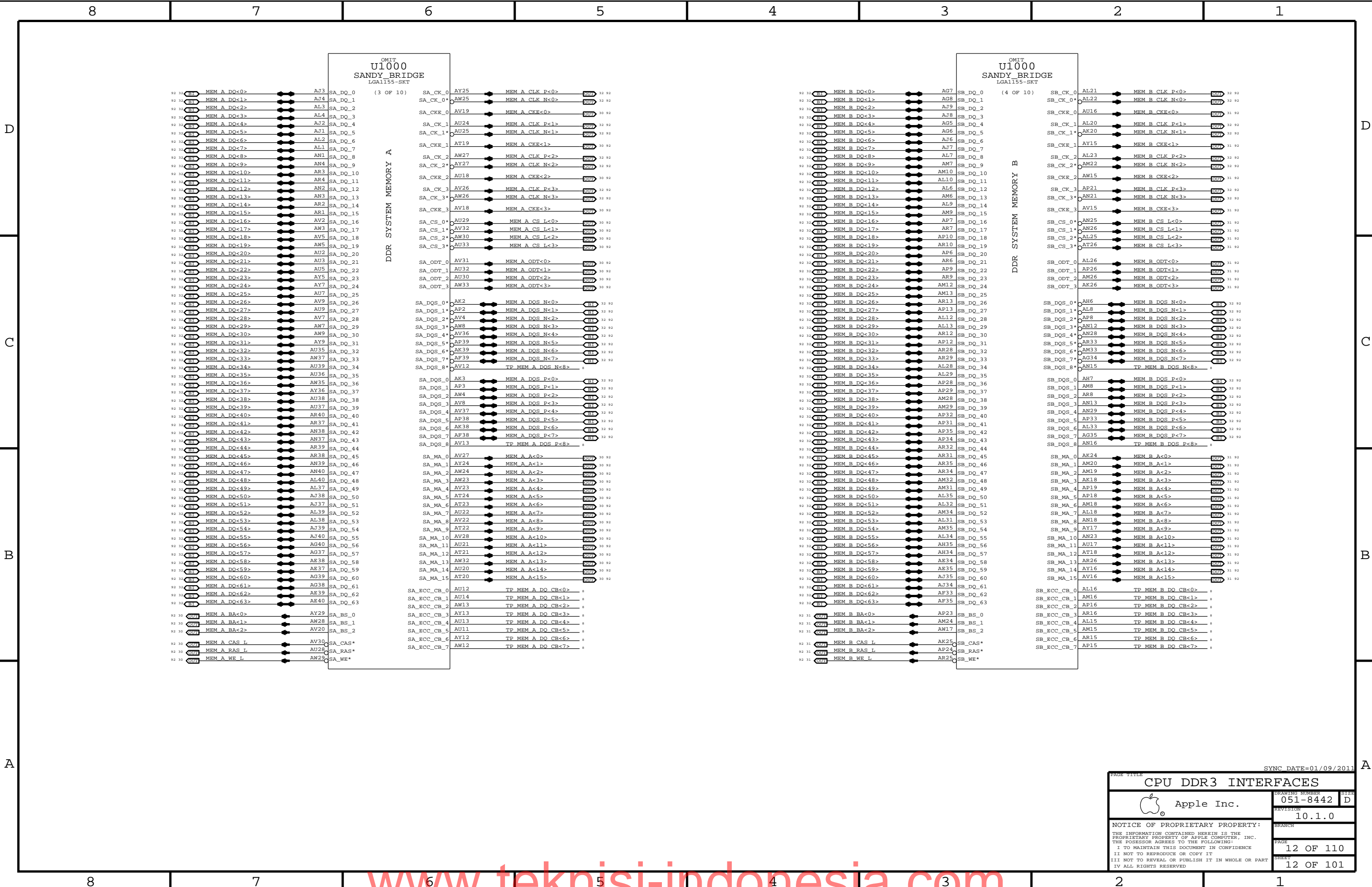
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8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1



| PAGE TITLE | | |
|---|----------------|-----------------|
| CPU CLOCK/MISC/JTAG | | |
|  Apple Inc. | DRAWING NUMBER | 051-8442 |
| | REVISION | 10.1.0 |
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| | | SHEET 11 OF 101 |



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DRAWING NUMBER

051-8442

REVISION

10.1.0

PAGE

12 OF 110

SHEET

12 OF 101

SIZE

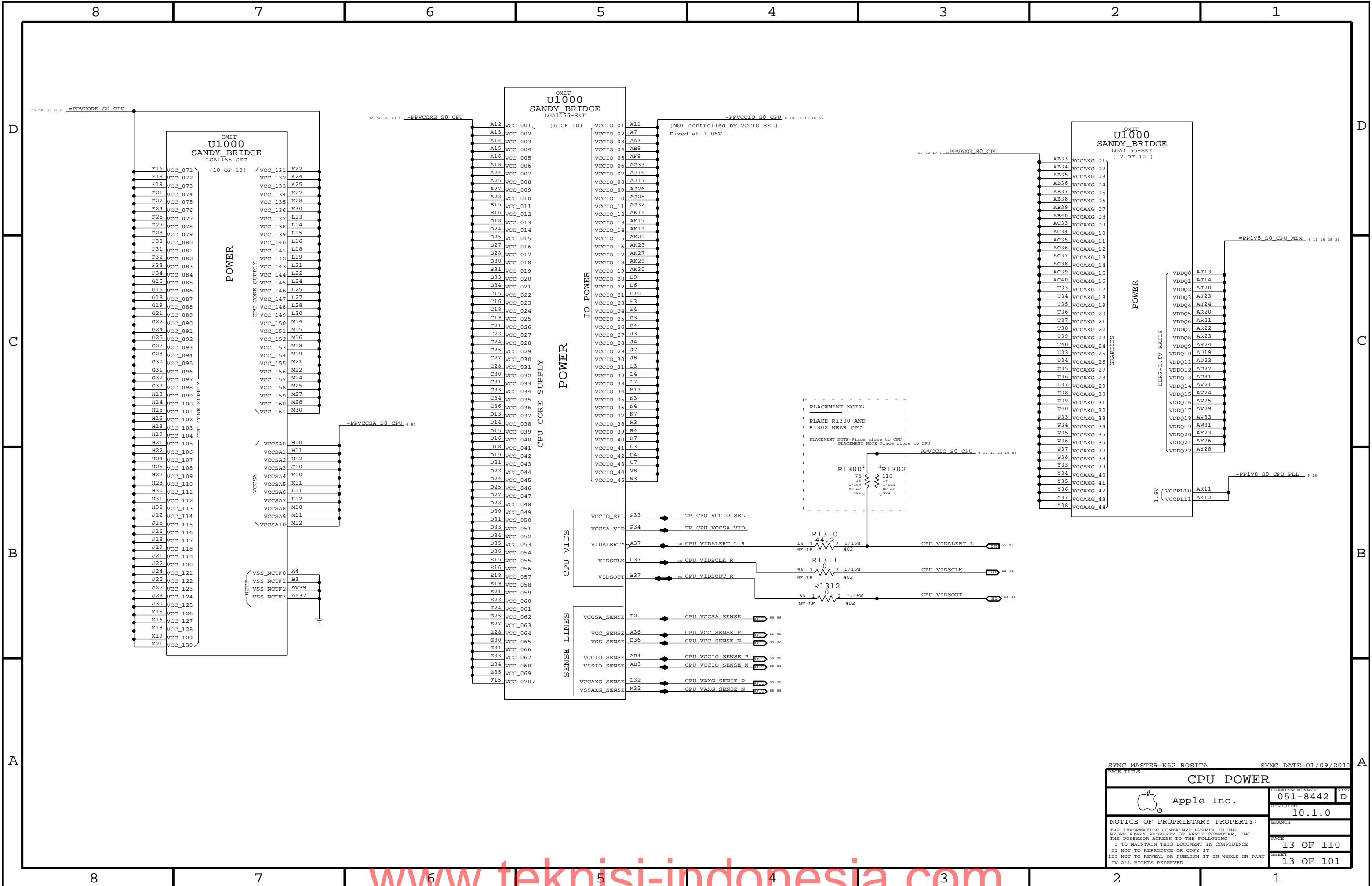
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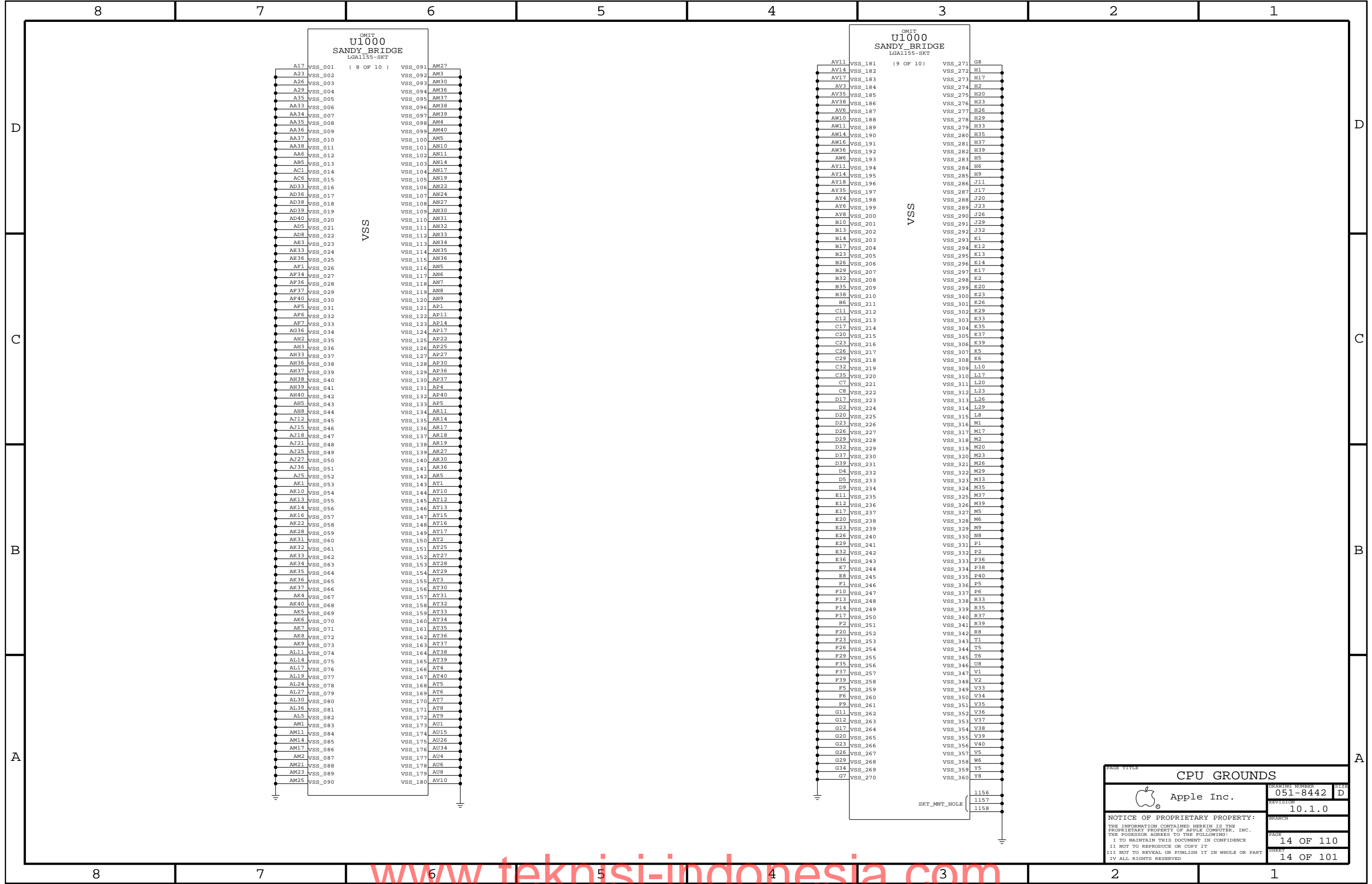
CPU DDR3 INTERFACES


SYNC DATE=01/09/2011

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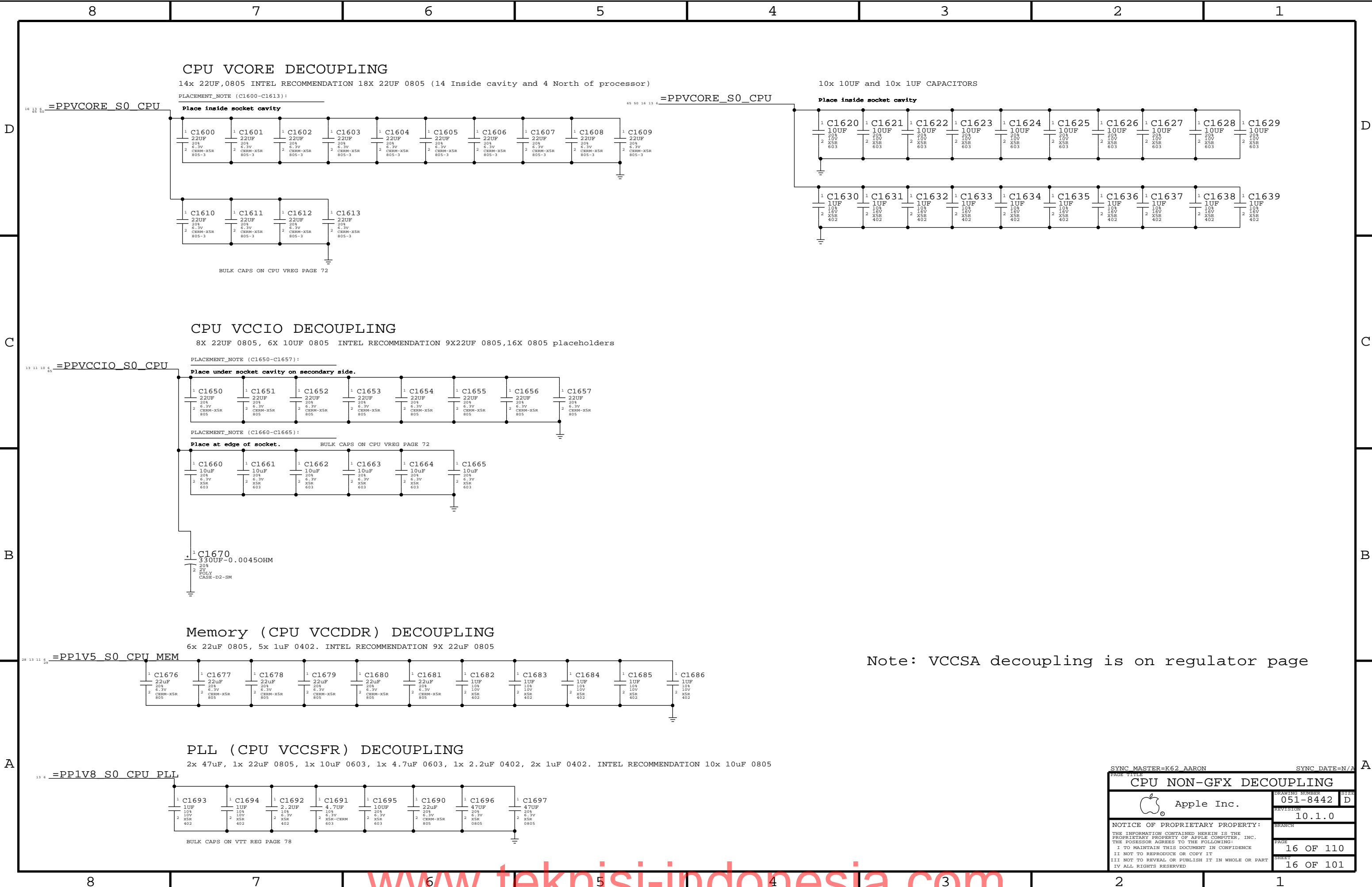


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|---|--|----------------|--|-----------|--|
| PAGE TITLE | | DRAWING NUMBER | | SIZE | |
| CPU POWER | | 051-8442 | | D | |
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| PAGE TITLE | | | |
|---|----------------|-----------|-----------|
| CPU GROUNDS | | | |
|  Apple Inc. | DRAWING NUMBER | 051-8442 | SIZE D |
| | REVISION | 10.1.0 | |
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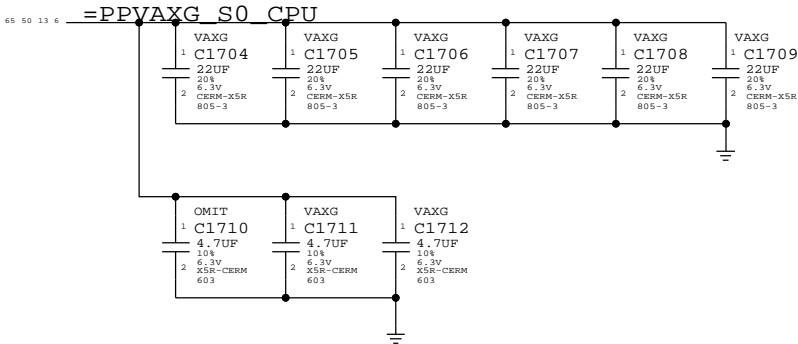


VAXG DECOUPLING

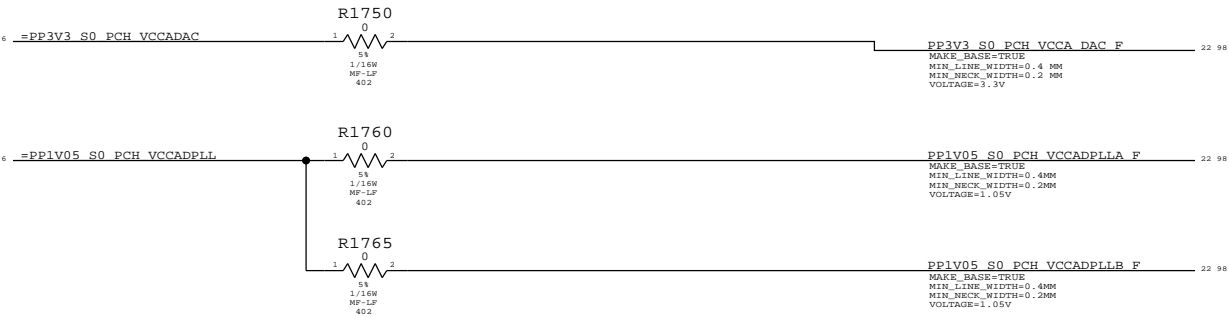
INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|-------------------------|-------------------------|------------|
| 138S0586 | 1 | CAP,4.7UF,10%,6.3V,0603 | C1710 | VAXG |
| 113S0022 | 1 | RES,0 OHM,5%,0603 | C1710 | NO_VAXG |



SYNC MASTER=K62 AARON

SYNC DATE=11/30/2009

GFX DECOUPLING & PCH PWR ALIAS

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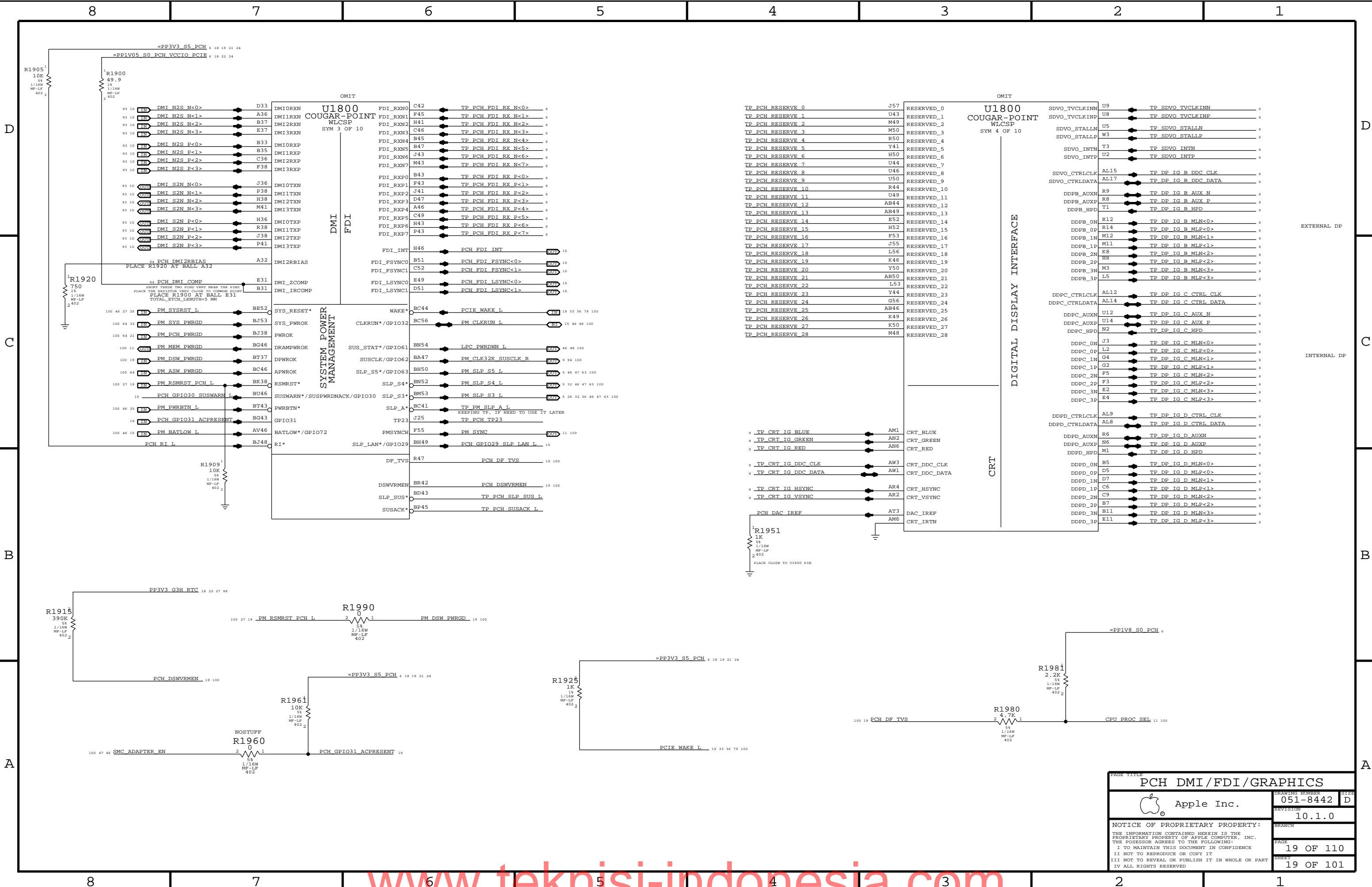
17 OF 110

SHEET

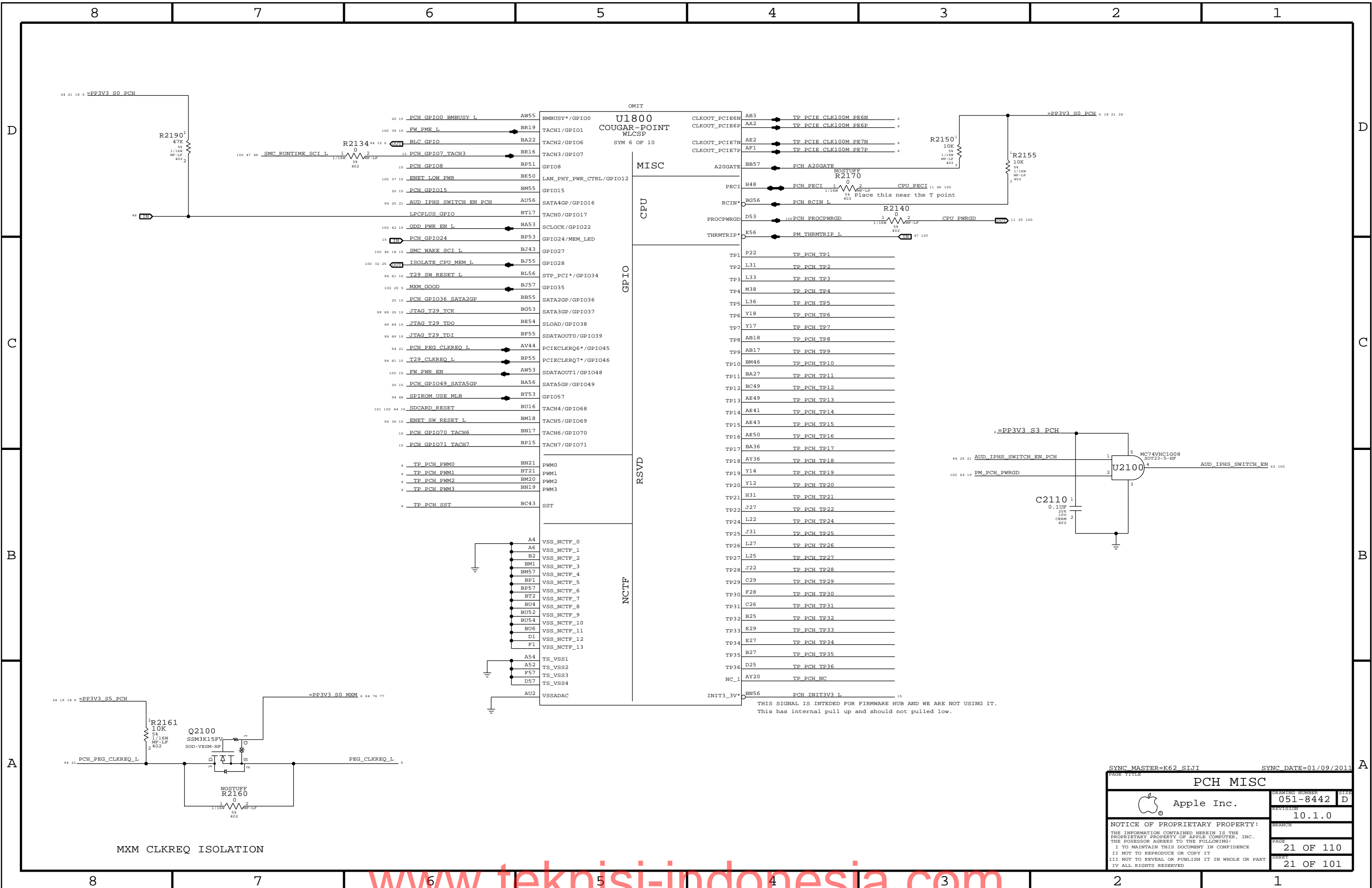
17 OF 101

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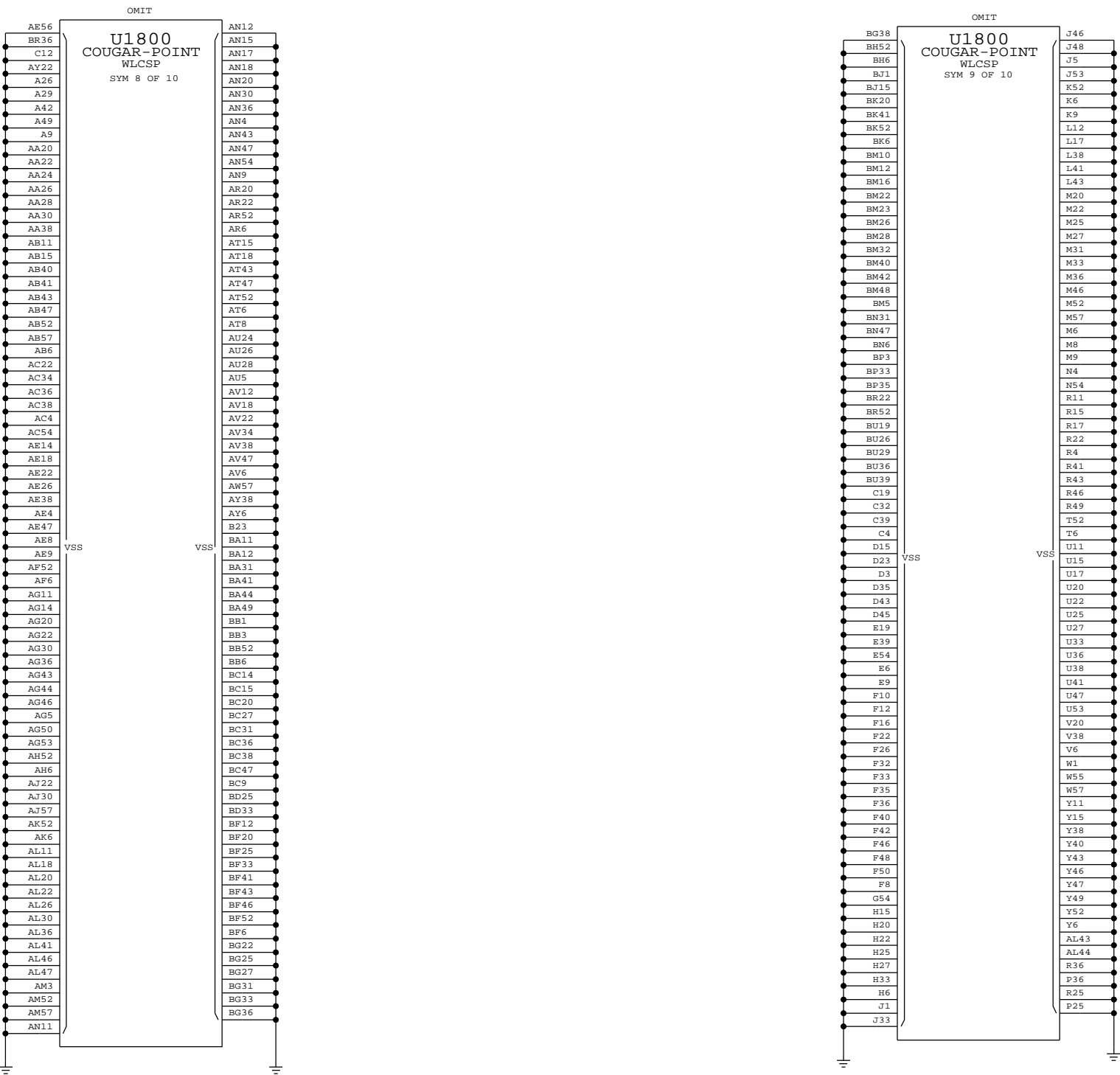
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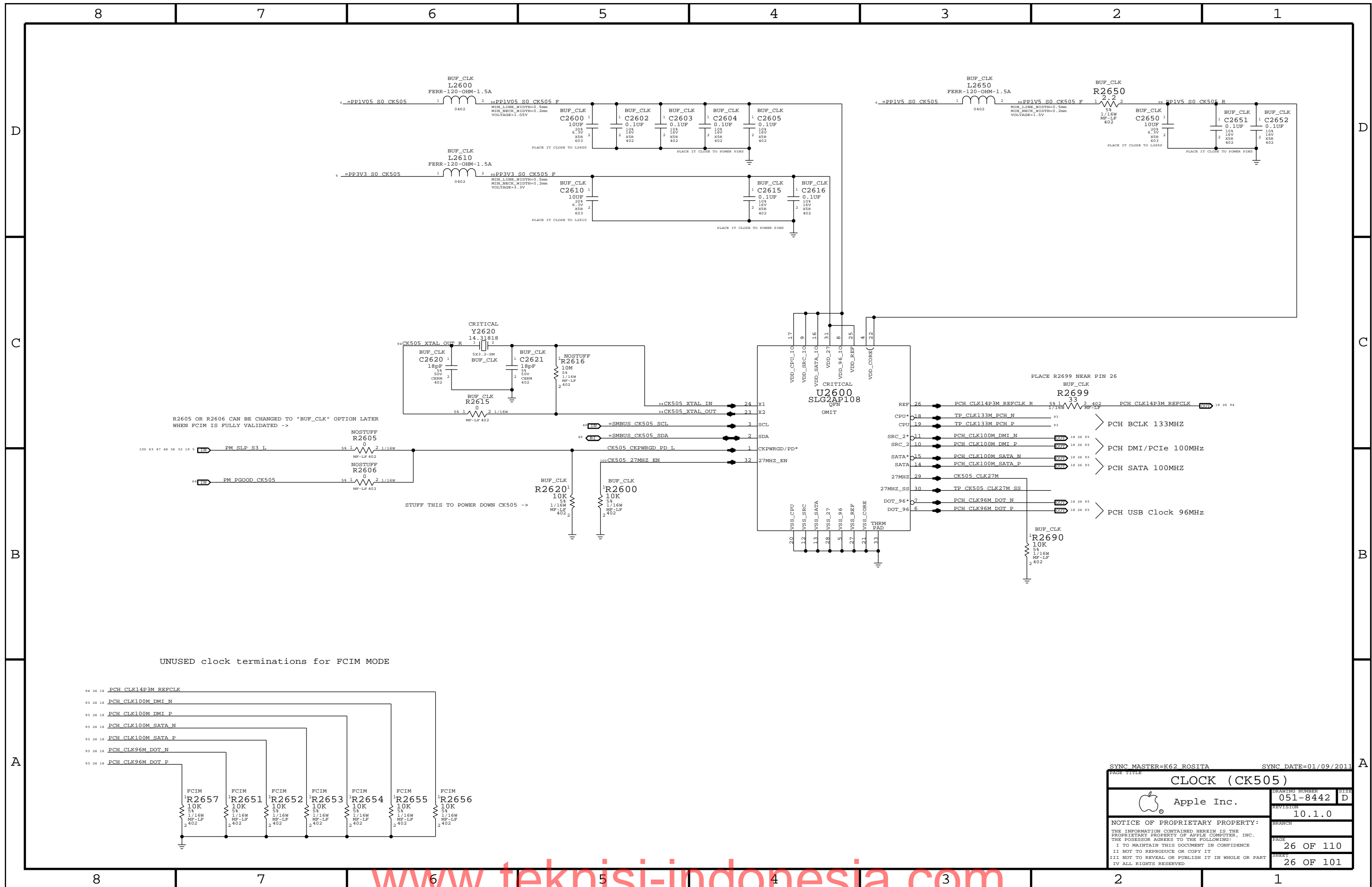
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SYNC DATE=07/01/2009

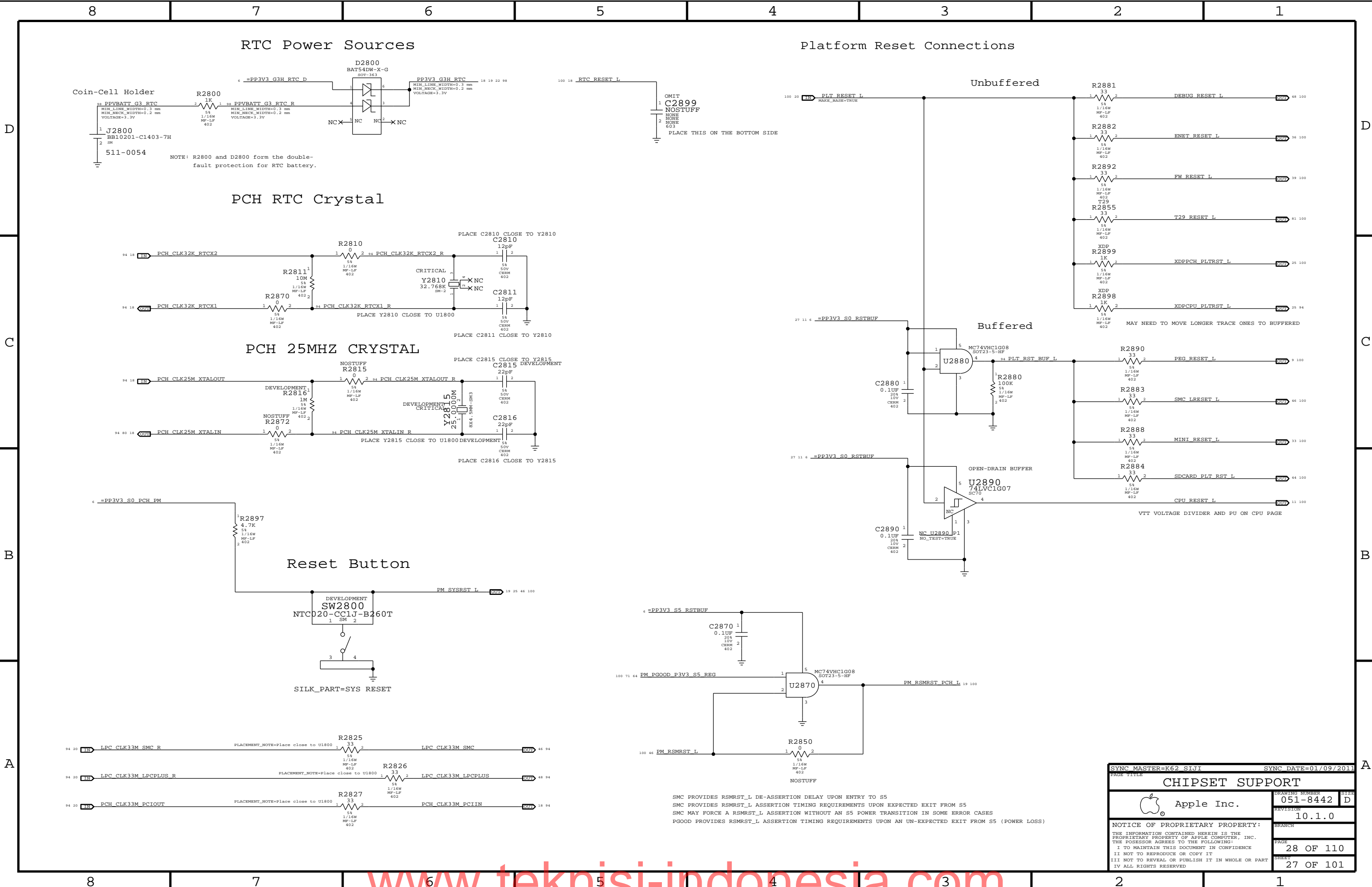
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|---|----------------|-------------|------|
| PAGE TITLE | | PCH GROUNDS | |
|  Apple Inc. | DRAWING NUMBER | 051-8442 | SIZE |
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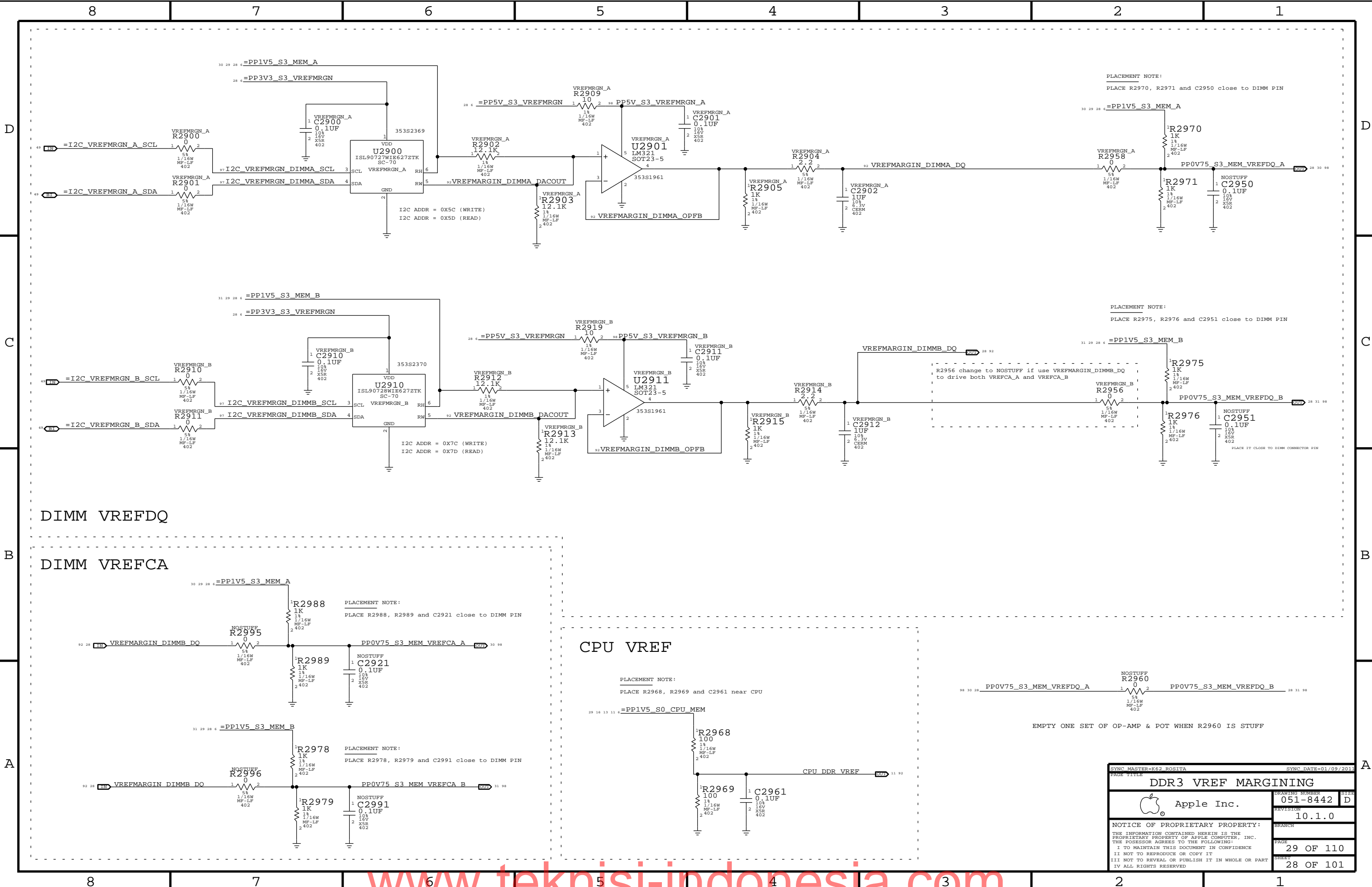




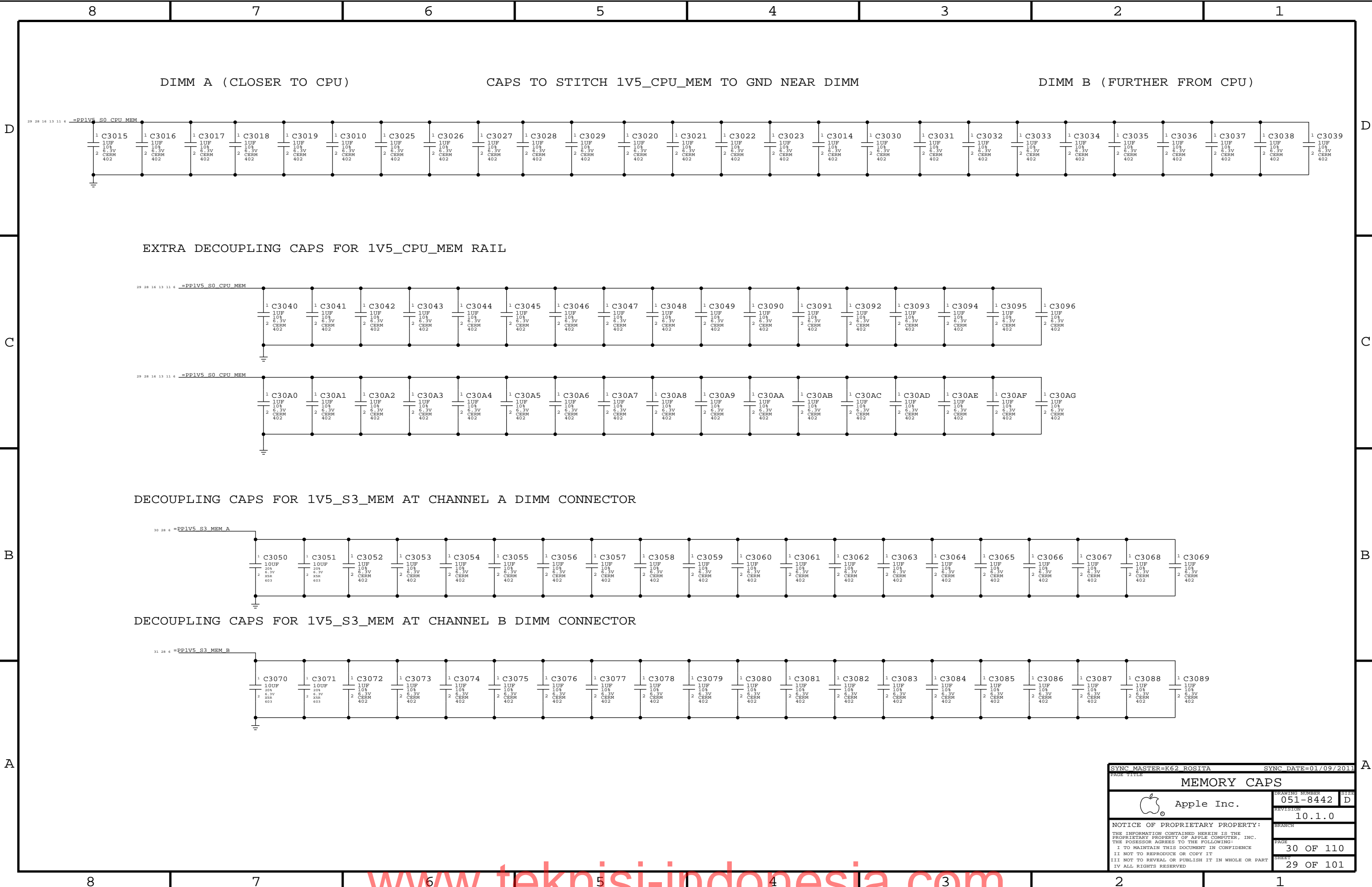
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|---|------------|----------------------|-----------|
| SYNC MASTER=K62 ROSITA | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| CLOCK (CK505) | | | |
|  | Apple Inc. | DRAWING NUMBER | 051-8442 |
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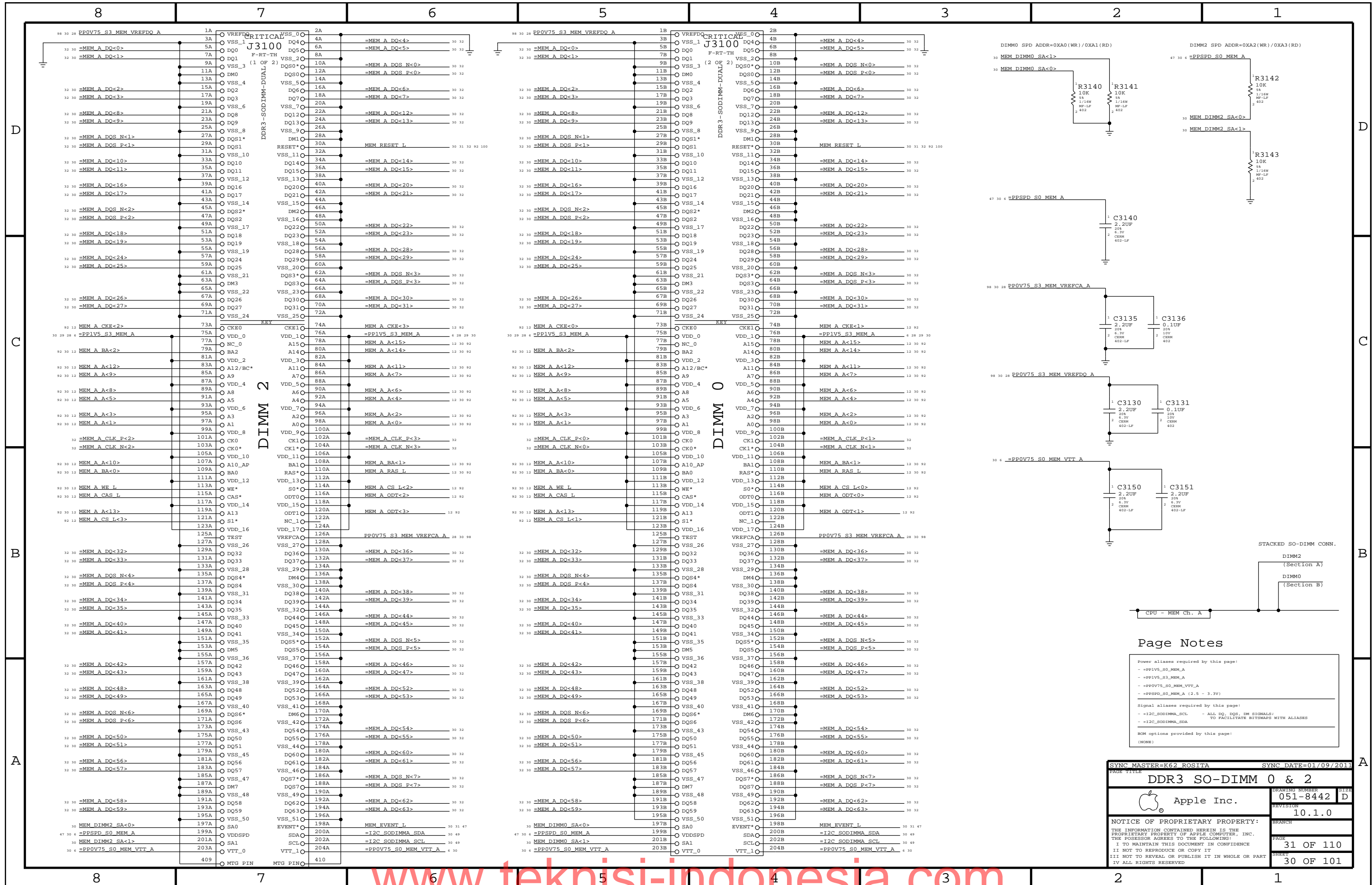
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|---|--|----------------------|--|----------------------|--|
| PAGE TITLE | | SYNC MASTER=K62_S1J1 | | SYNC DATE=01/09/2011 | |
| CHIPSET SUPPORT | | DRAWING NUMBER | | SIZE | |
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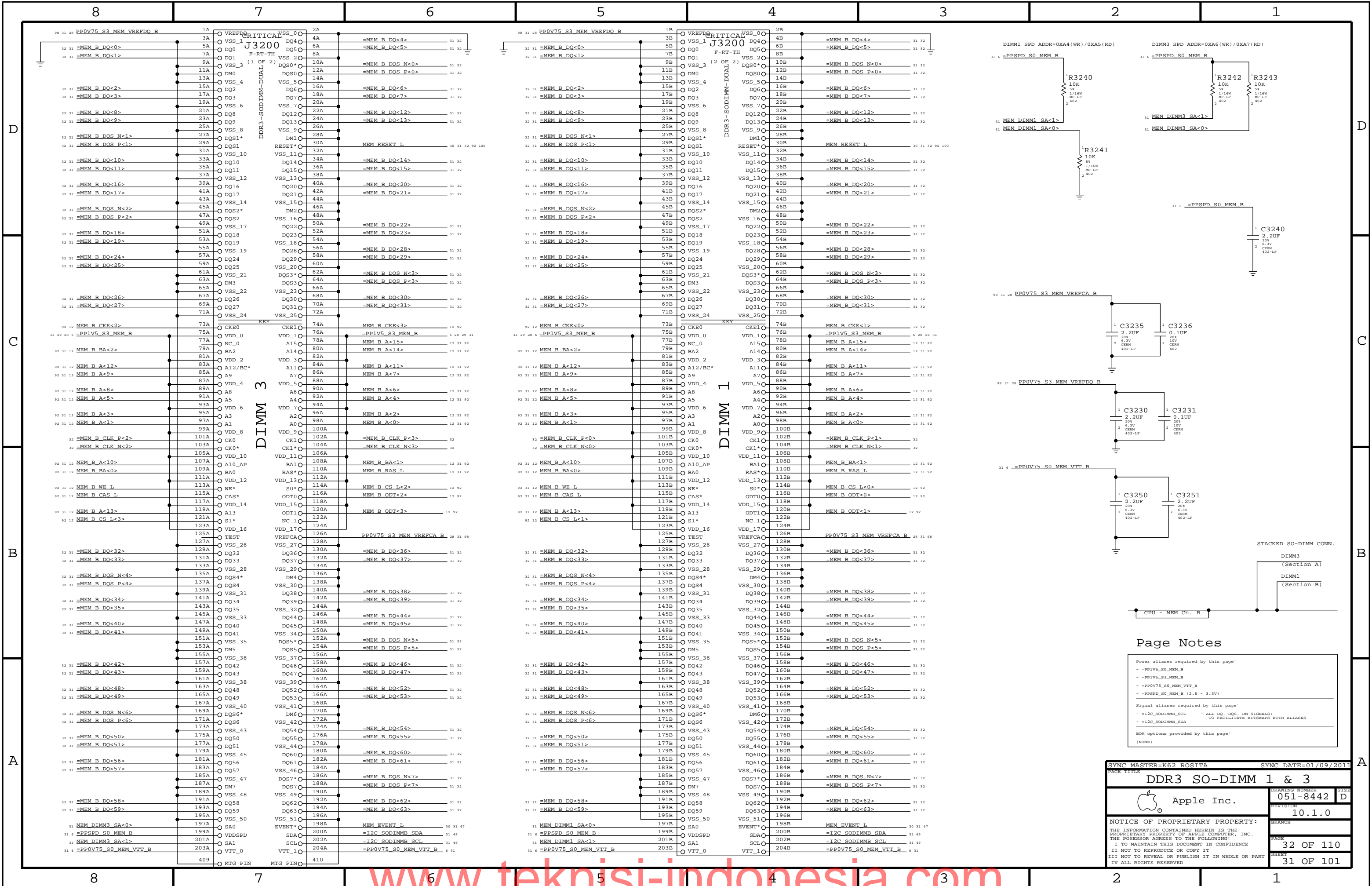


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|---|--|----------------------|-----------|
| SYNC MASTER=K62 ROSITA | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | DDR3 VREF MARGINING | |
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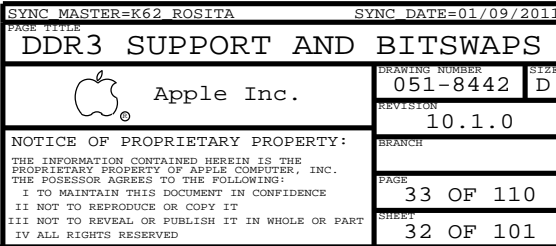
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| SYNC MASTER=K62 ROSITA | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| MEMORY CAPS | | | |
|  Apple Inc. | DRAWING NUMBER | | SHEET |
| | 051-8442 | | D |
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| | | 30 OF 110 | |
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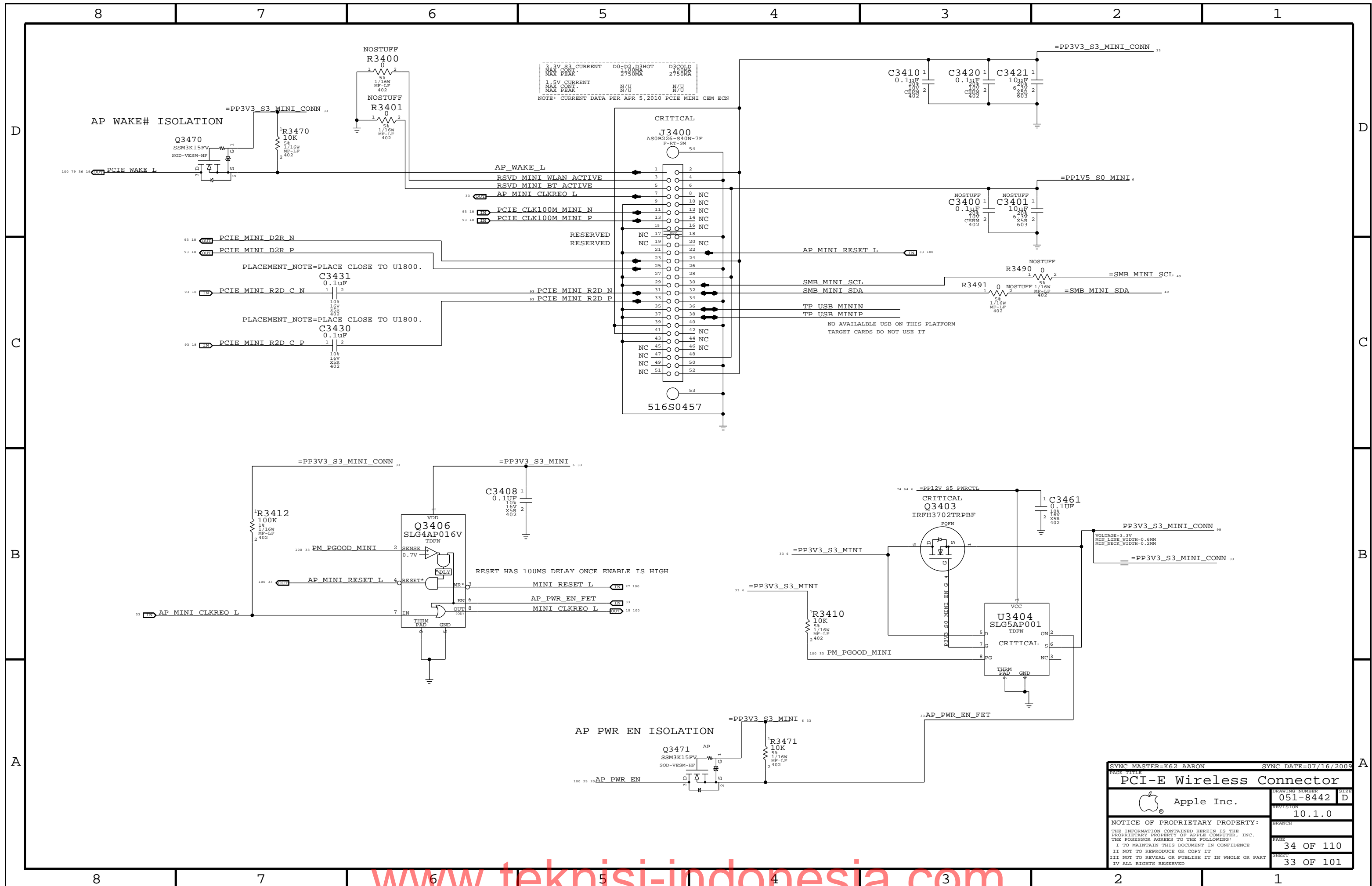





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SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.





| | | | |
|---|--|----------------------|-----------|
| SYNC MASTER=K62 AARON | | SYNC DATE=07/16/2009 | |
| PAGE TITLE | | | |
| PCI-E Wireless Connector | | | |
|  Apple Inc. | | DRAWING NUMBER | 051-8442 |
| | | SIZE | D |
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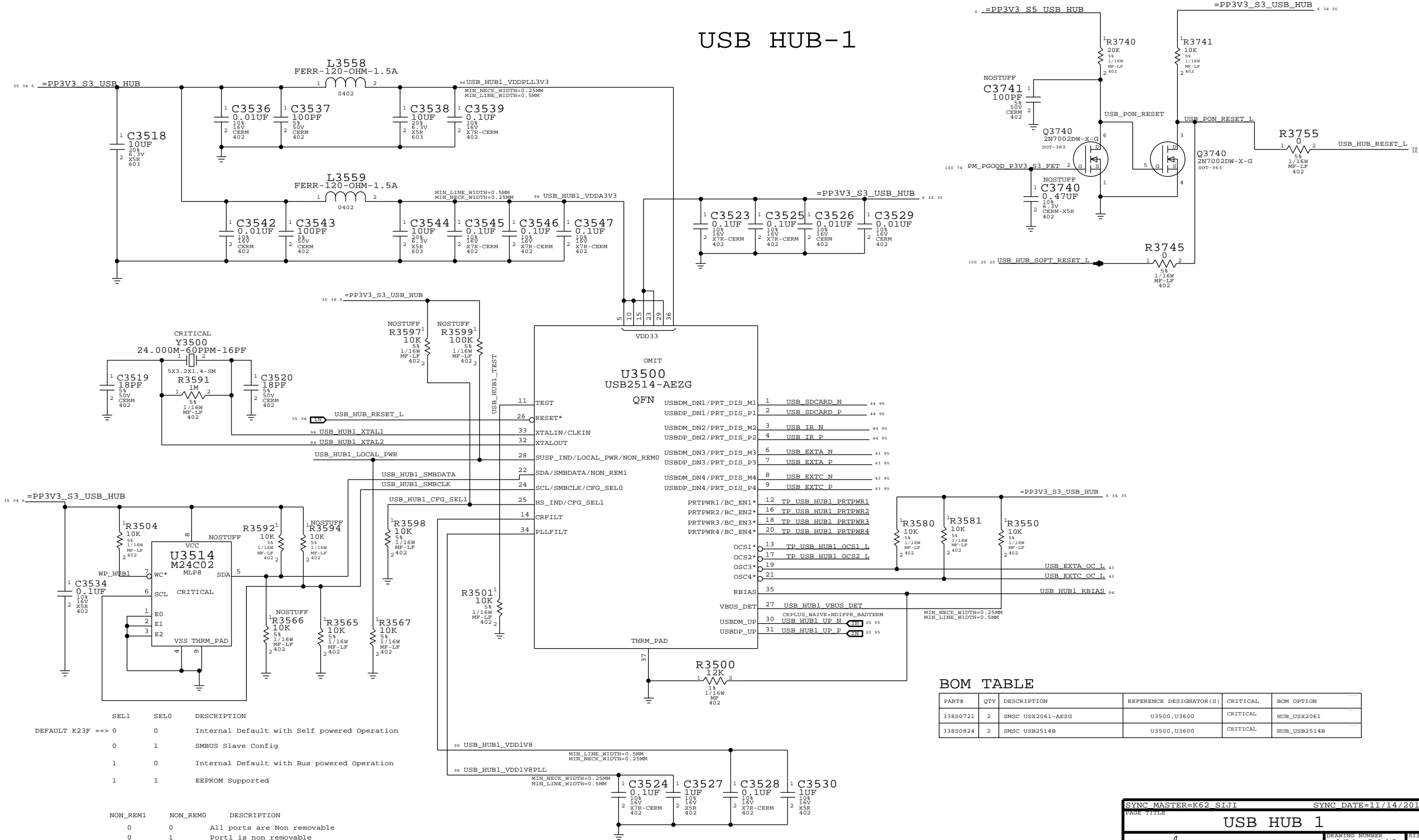
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USB HUB-1



BOM TABLE

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-------------------|-------------------------|----------|--------------|
| 338S0721 | 2 | SMSC USX2061-AEZG | U3500,U3600 | CRITICAL | HUB_USX2061 |
| 338S0824 | 2 | SMSC USB2514B | U3500,U3600 | CRITICAL | HUB_USB2514B |

| SEL1 | SEL0 | DESCRIPTION |
|--------------------|------|--|
| DEFAULT K23F ==> 0 | 0 | Internal Default with Self powered Operation |
| 0 | 1 | SMBUS Slave Config |
| 1 | 0 | Internal Default with Bus powered Operation |
| 1 | 1 | EEPROM Supported |

| NON_REM1 | NON_REMO | DESCRIPTION |
|--------------------|----------|---------------------------------|
| 0 | 0 | All ports are Non removable |
| 0 | 1 | Port1 is non removable |
| DEFAULT K23F ==> 1 | 0 | Port 1 and 2 are non removable |
| 1 | 1 | Port1,2 and 3 are non Removable |

SYNC MASTER=K62_S1J1

SYNC DATE=11/14/2010

USB HUB 1

Apple Inc.

DRAWING NUMBER

051-8442

SIZE

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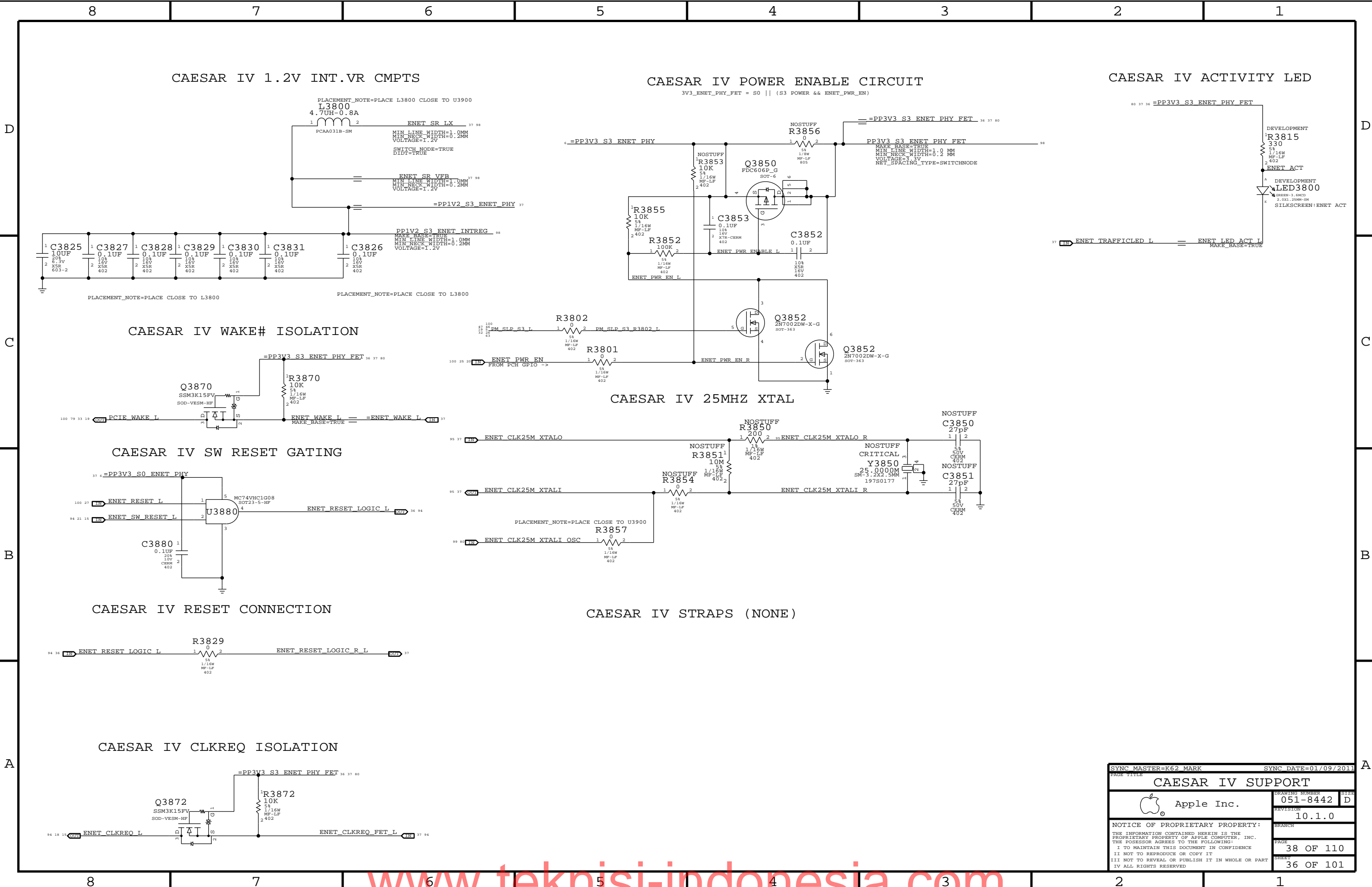
SHEET


34 OF 101

The image shows a complex PCB layout for a USB hub. The layout is divided into several functional blocks:

- Power and Ground Planes:** The top and bottom of the layout are dominated by power and ground planes, with various decoupling capacitors (C3618, C3636, C3637, C3638, C3639, C3642, C3643, C3644, C3645, C3646, C3647, C3623, C3625, C3626, C3629) placed to filter noise and provide stable power.
- USB Hub Controller (U3600):** The central component is the U3600 USB2514-AEZG, which is connected to the USB hub pins (1-16) and provides control signals to the other components.
- USB Hub Controller (U3614):** The U3614 M24C02 is a non-volatile memory device used for storing configuration data. It is connected to the USB hub controller and provides a stable memory source.
- USB Hub Controller (U3629):** The U3629 is a USB hub controller that provides additional control and monitoring functions. It is connected to the USB hub controller and provides control signals to the other components.
- Resistors and Pull-ups:** Numerous resistors (R3604, R3692, R3694, R3698, R3601, R3665, R3666, R3667, R3660, R3661, R3680, R3681, R3682) are used to provide pull-up and pull-down functions to the USB hub pins and control signals.
- Test Points and Jumper:** The layout includes several test points (TP USB HUB2 PRT PWR1, TP USB HUB2 PRT PWR2, TP USB HUB2 PRT PWR3, TP USB HUB2 PRT PWR4, TP USB HUB2 OCS1, TP USB HUB2 OCS2, TP USB HUB2 OC L, TP USB HUB2 OC L, TP USB HUB2 RBIAS) and a jumper (J1) for configuration.
- Dimensions and Tolerances:** The layout is annotated with dimensions (e.g., 0.5mm, 0.25mm, 0.1mm) and tolerances (e.g., 0.5mm, 0.25mm, 0.1mm) to ensure accurate manufacturing.

| | | | |
|---|--|-----------------------|-----------|
| SYNCH MASTER=K62 SIJI | | SYNCH DATE=11/14/2010 | |
| PAGE TITLE | | | |
| USB HUB 2 | | | |
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| | | SHEET | 35 OF 101 |



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| SYNC MASTER=K62 MARK | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| CAESAR IV SUPPORT | | | |
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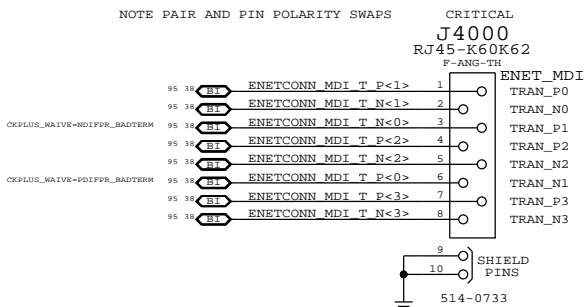
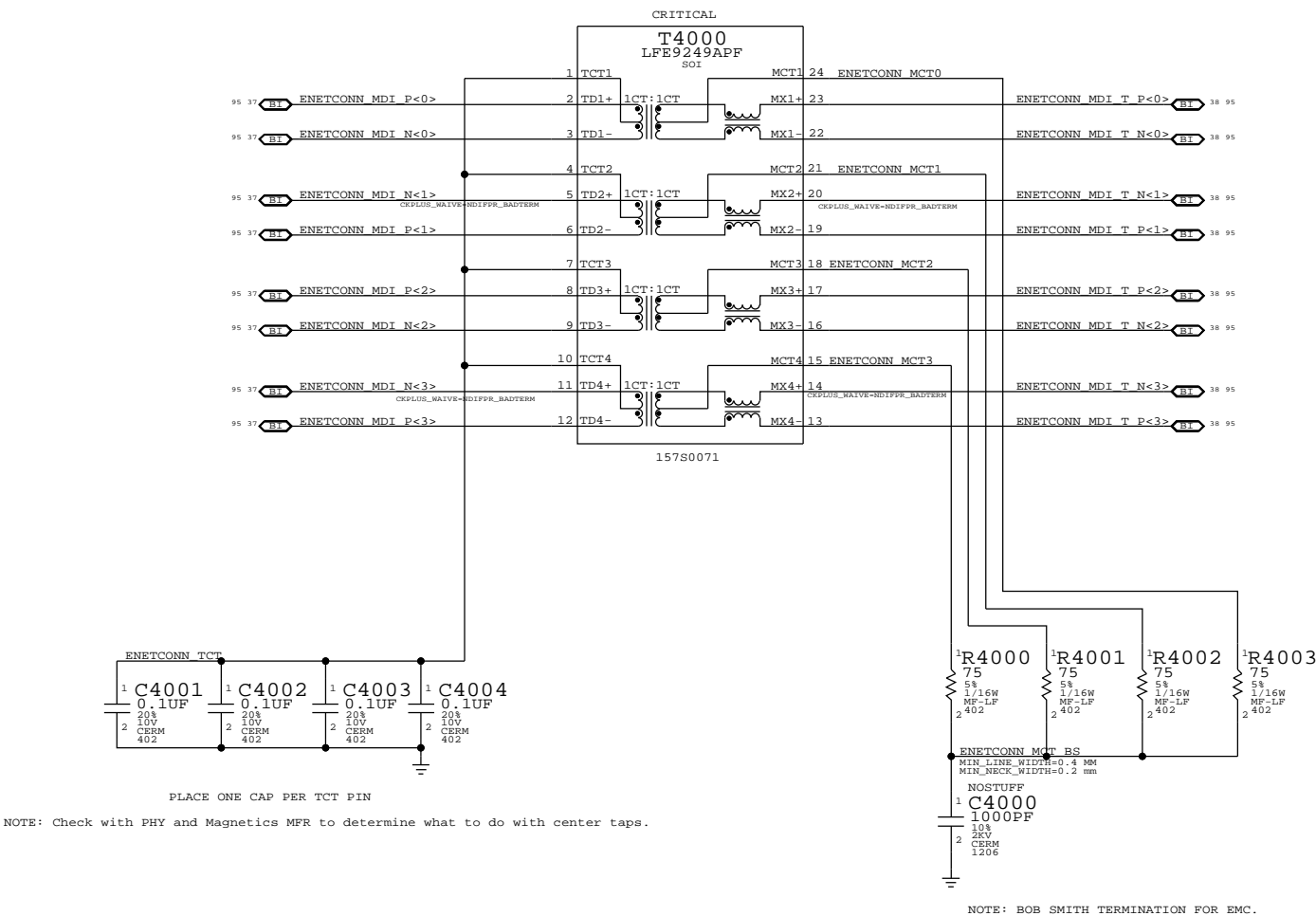
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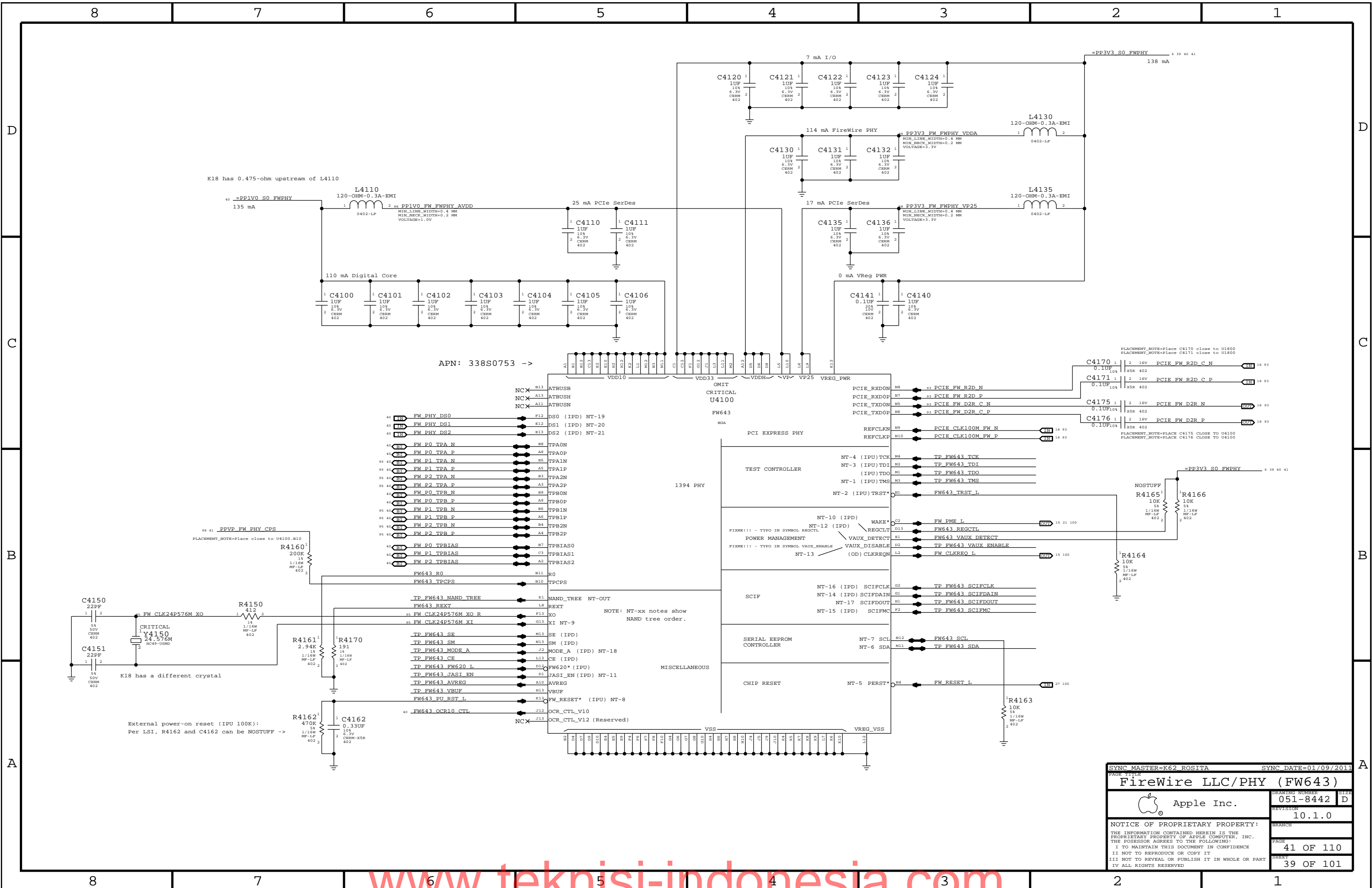
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THIS PAGE IS DIFFERENT BETWEEN K60 AND K62.



| | | | |
|---|--|----------------------|-----------|
| SYNC MASTER=K62 MARK | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| Ethernet Connector | | | |
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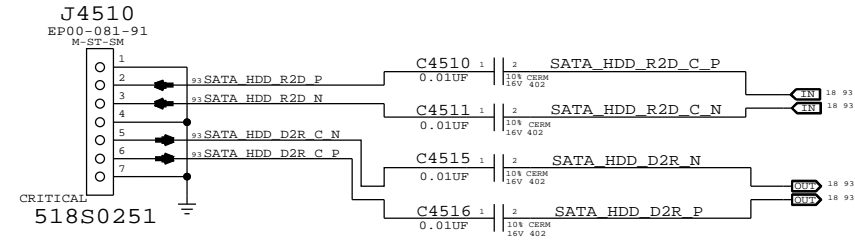
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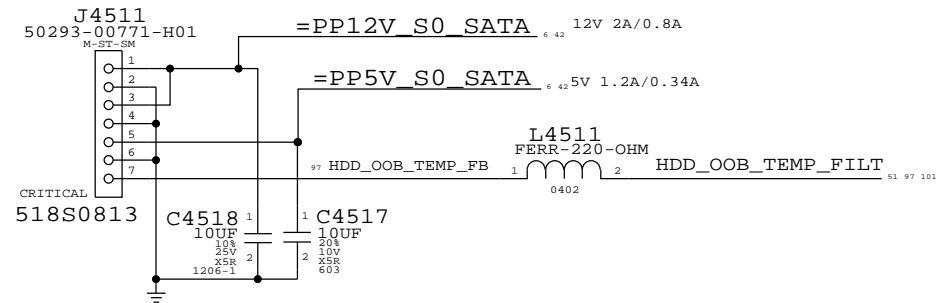
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SATA PORT A0 FOR HDD



SILKSCREEN:HDD PWR

HDD Power

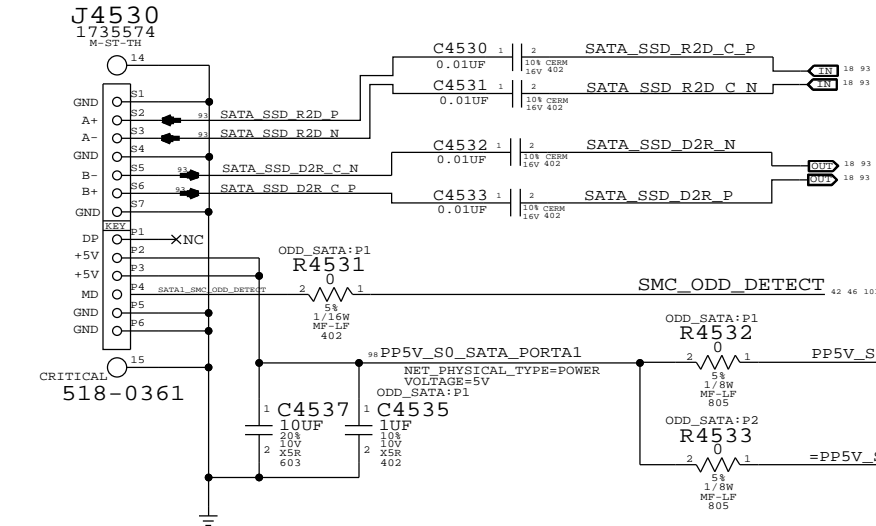


BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

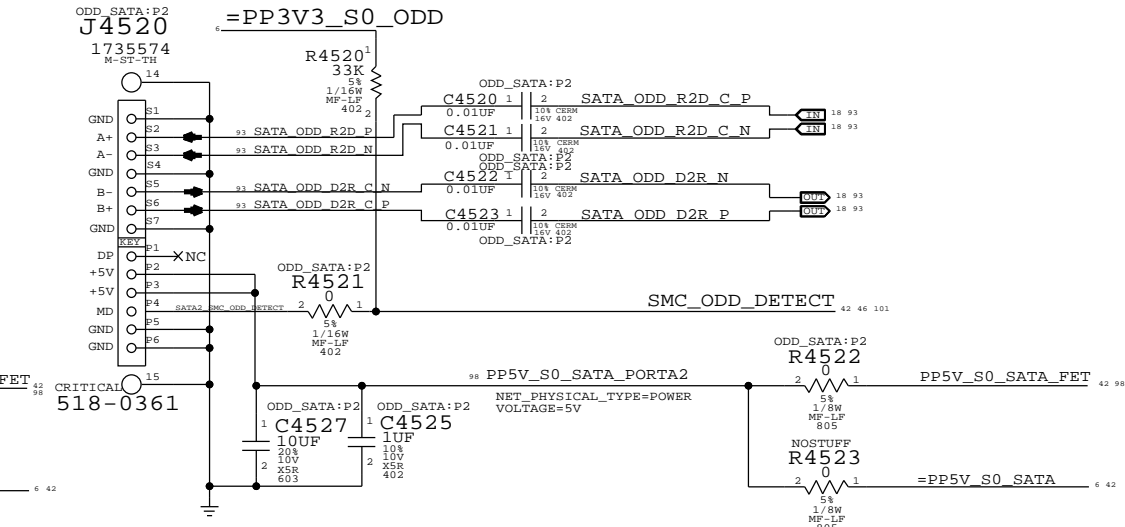
| A1 | A2 | ODD_SATA:P1 | ODD_SATA:P2 |
|-----|-----|-------------|-------------|
| SSD | ODD | | X |
| ODD | | X | |

SATA PORT A1 FOR SSD/ODD

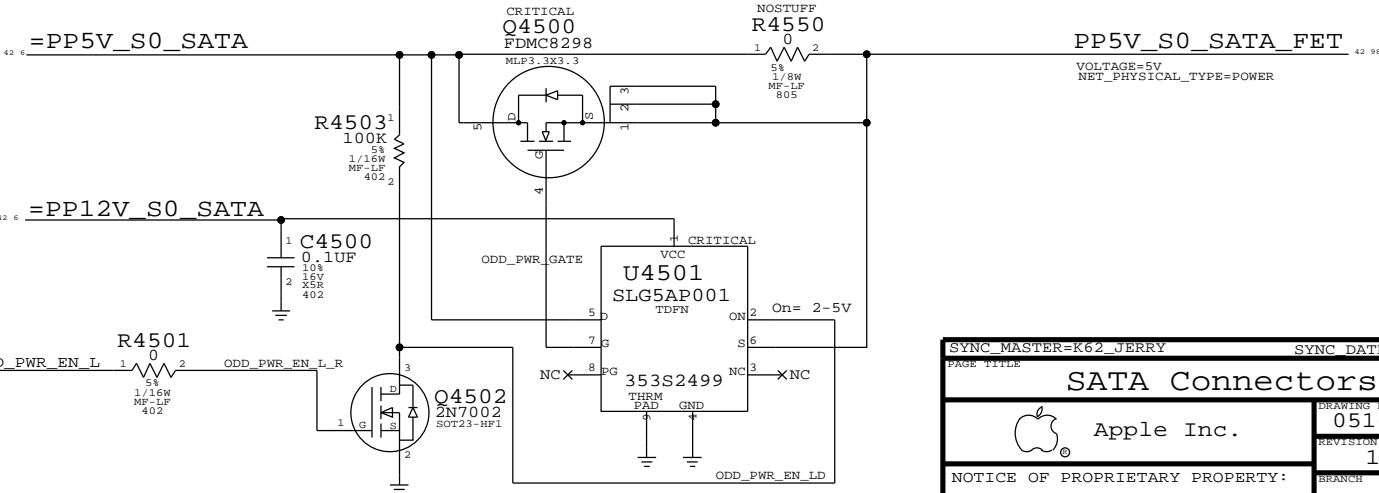
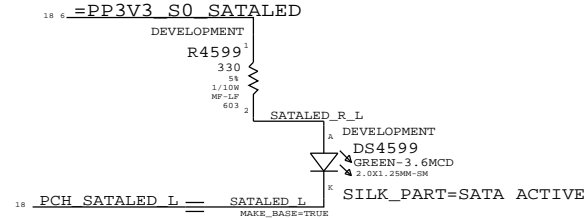
SILKSCREEN:SATA1



SILKSCREEN:SATA2



SATA Activity LED



| | | | |
|---|--|----------------------|-----------|
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| SATA Connectors | | DRAWING NUMBER | 051-8442 |
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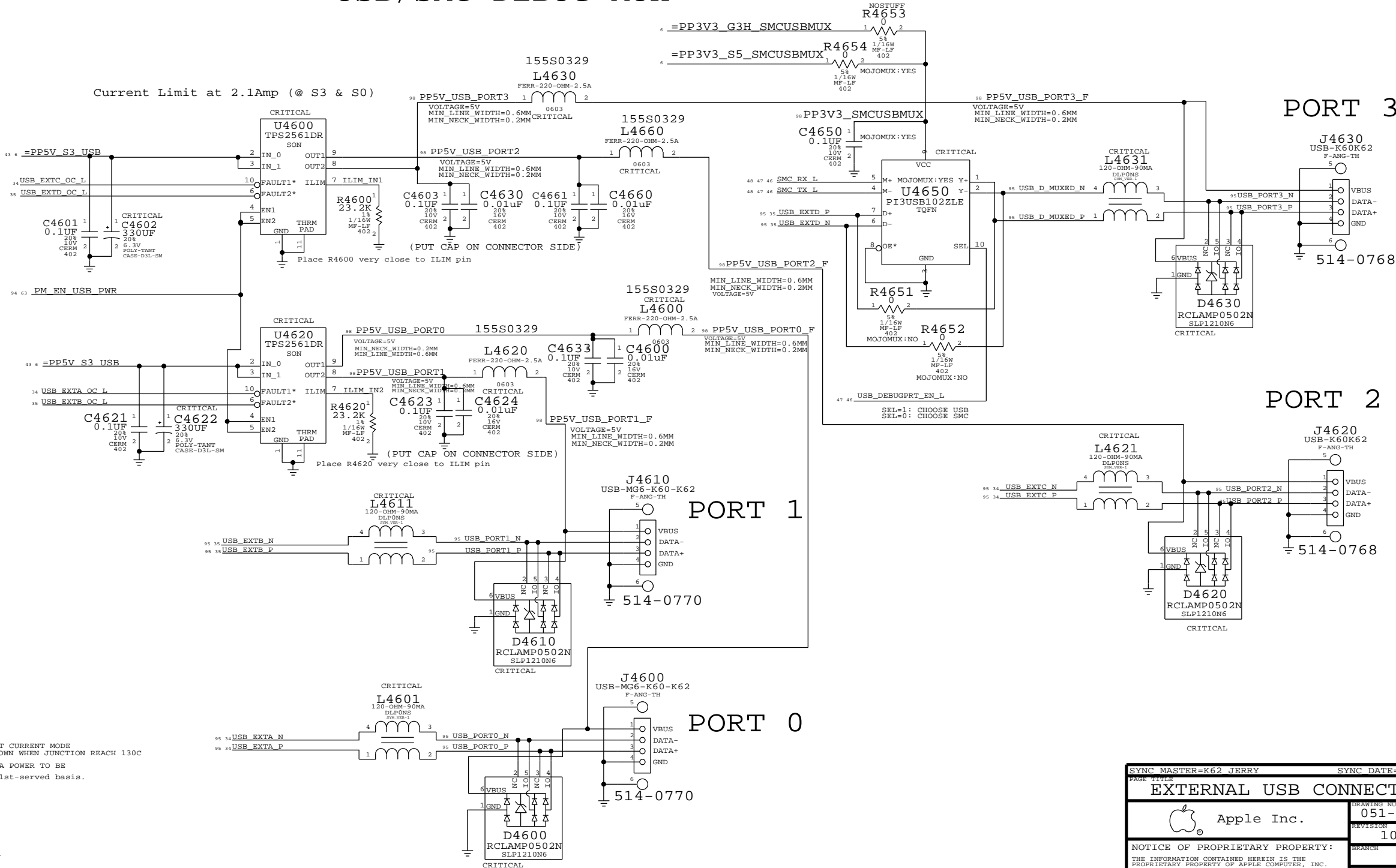
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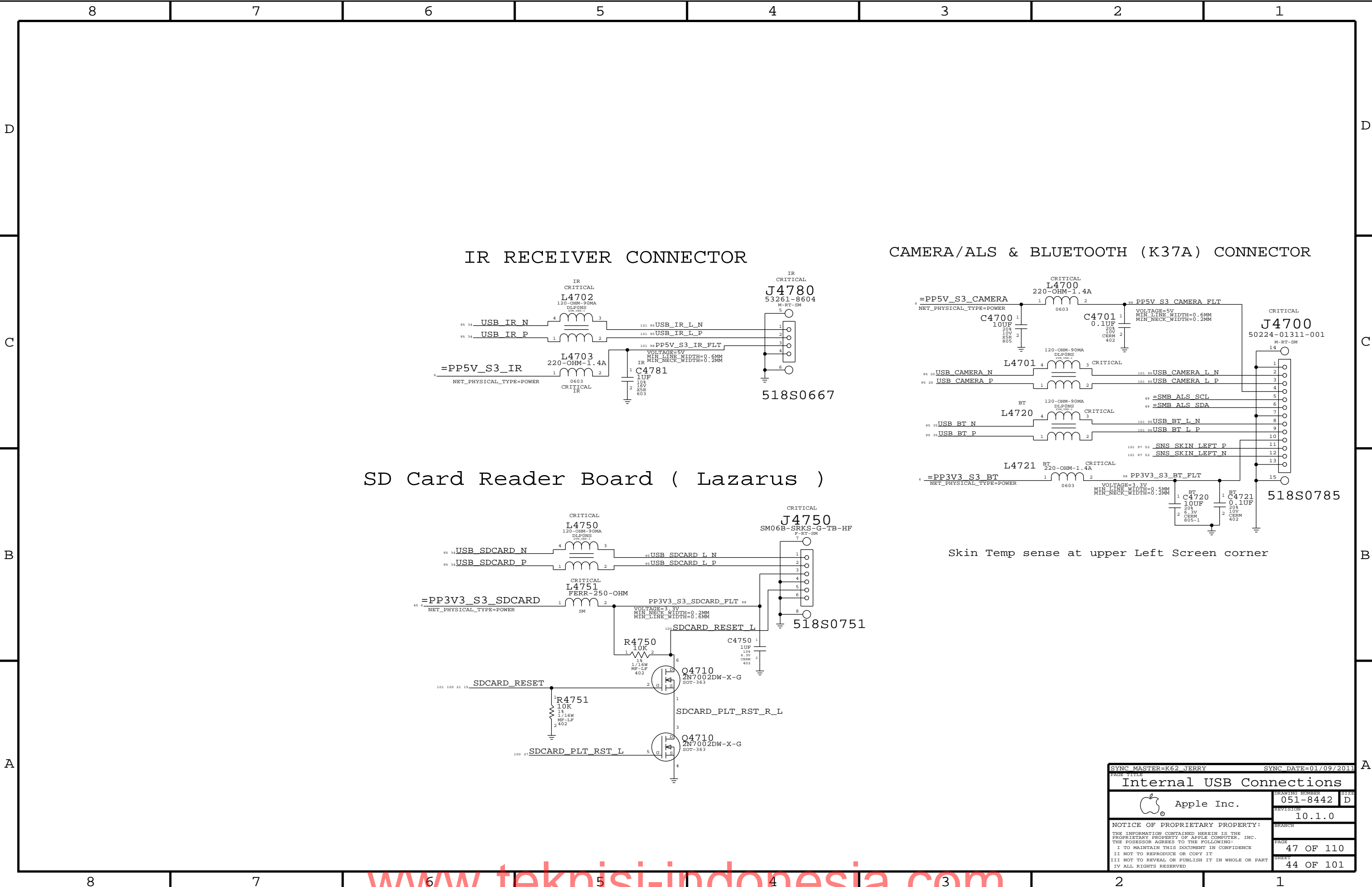
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USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL





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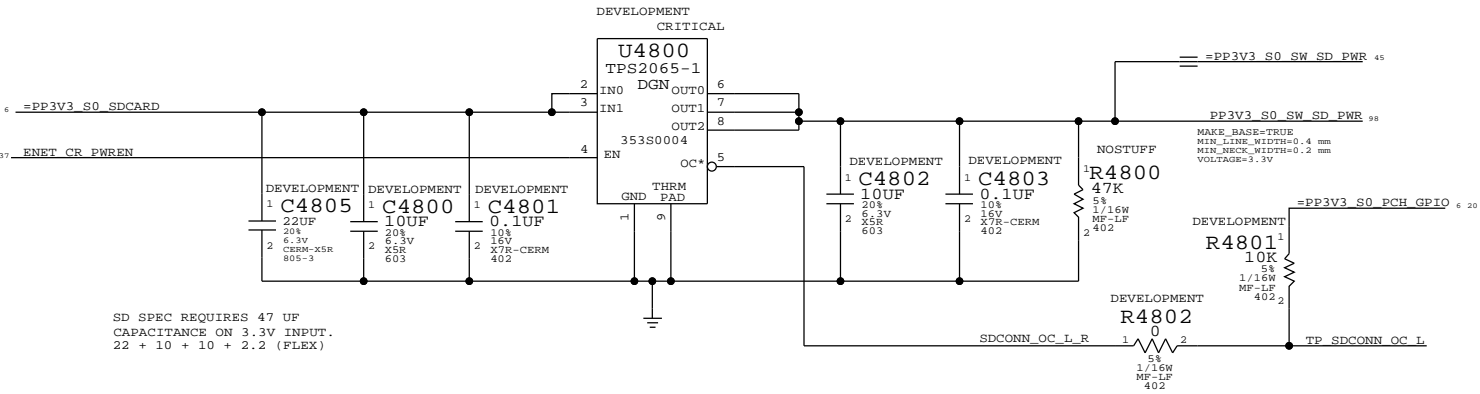
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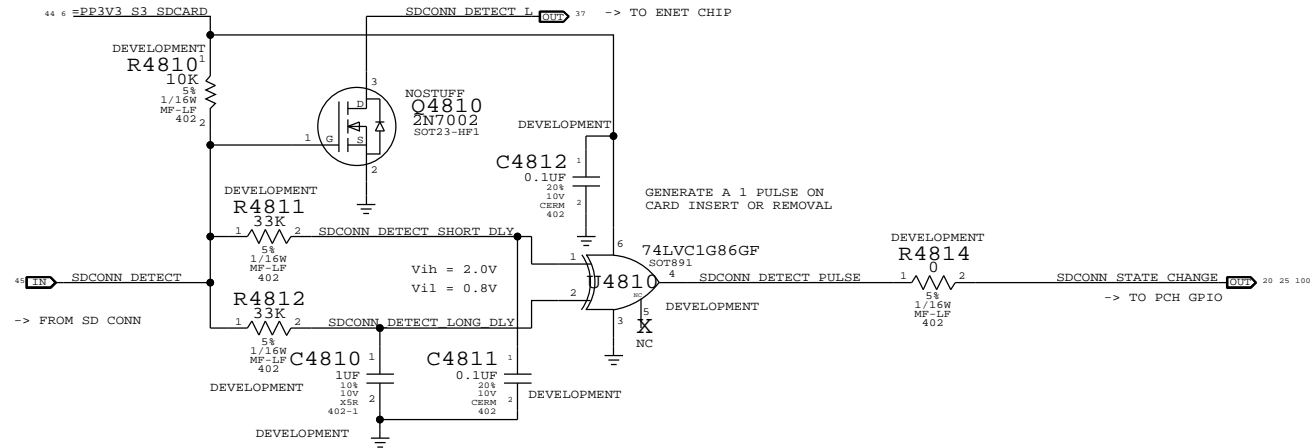
A

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

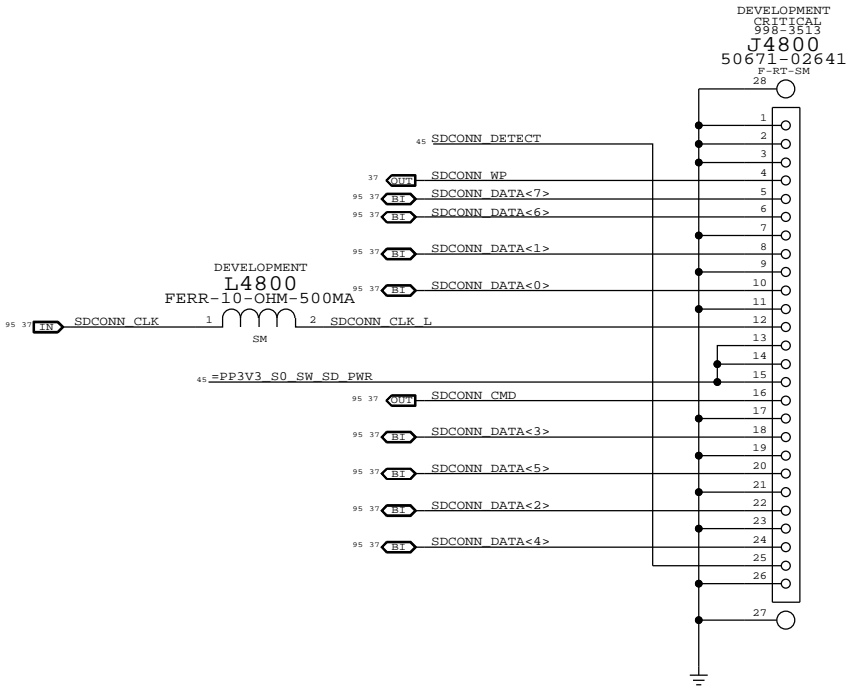
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.




SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



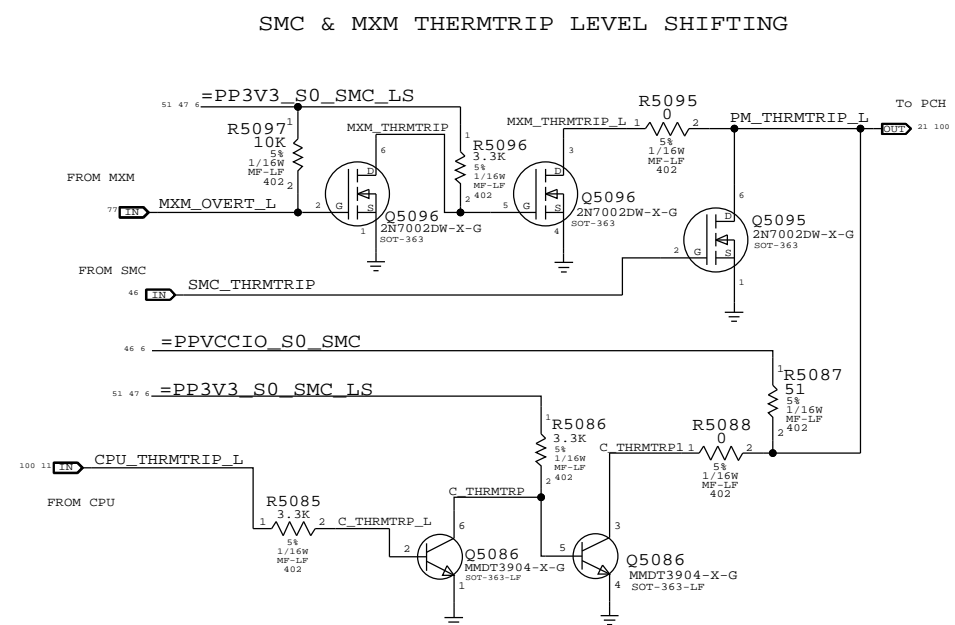
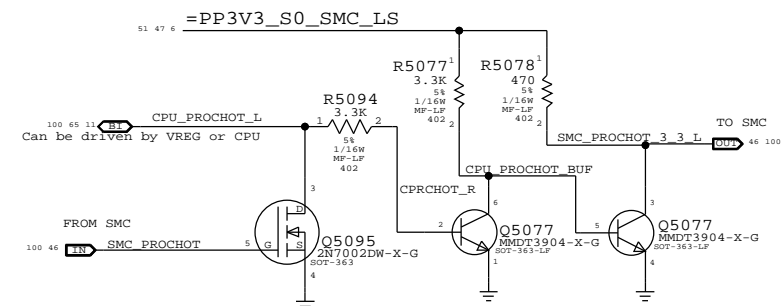
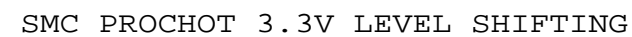
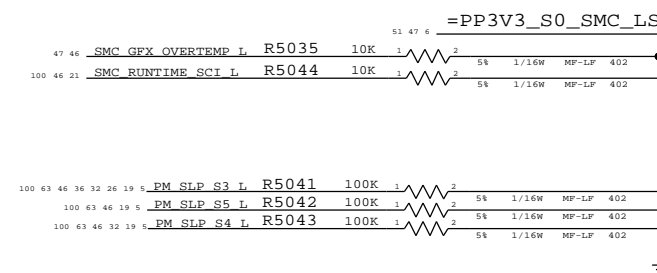
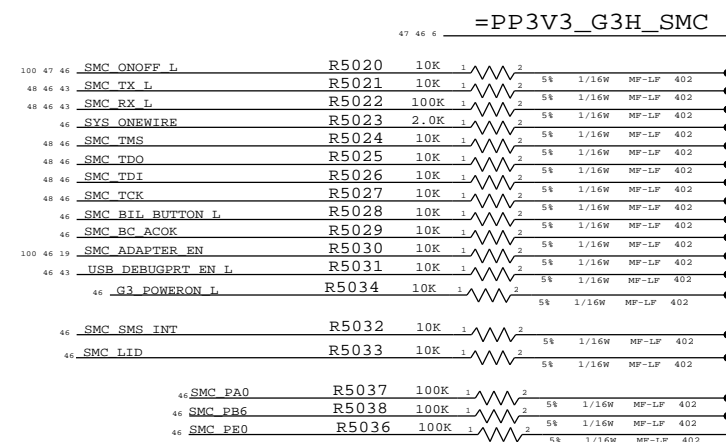
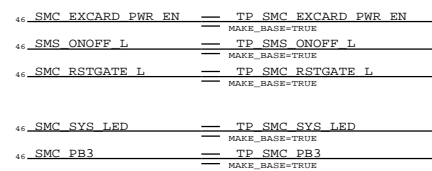
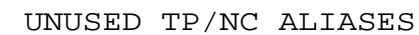
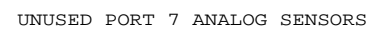
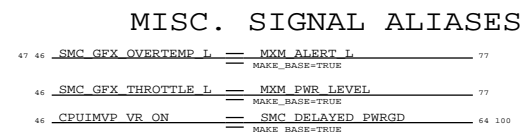
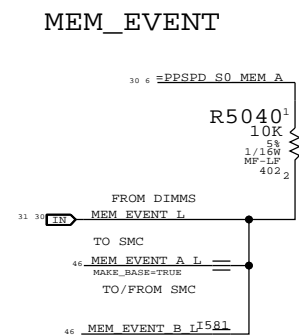
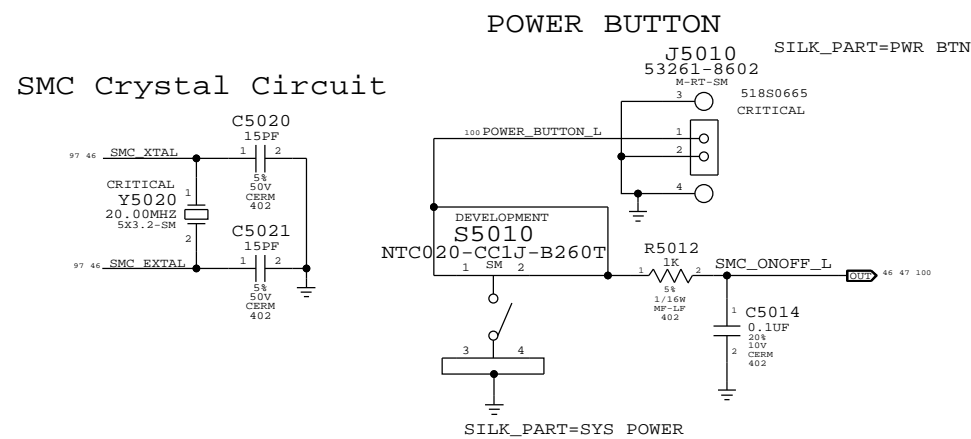
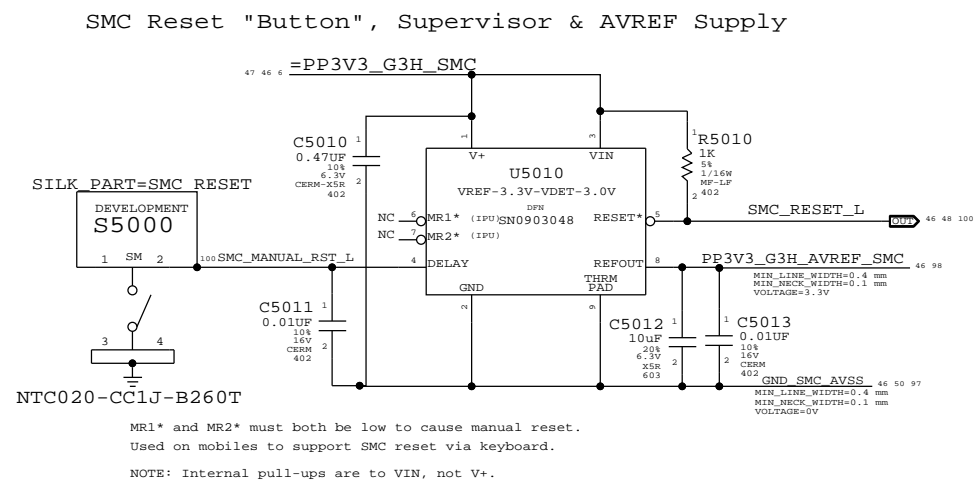
SD CARD CONNECTOR




(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

| | | | |
|---|--|----------------------|-----------|
| SYNC MASTER=K62 MARK | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| SD READER CONNECTOR | | | |
|  Apple Inc. | | DRAWING NUMBER | 051-8442 |
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| SYNC MASTER=K62 JERRY | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| SMC Support | | | |
|  Apple Inc. | DRAWING NUMBER | | SIZE |
| | 051-8442 | | D |
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| SHEET | | 47 OF 101 | |

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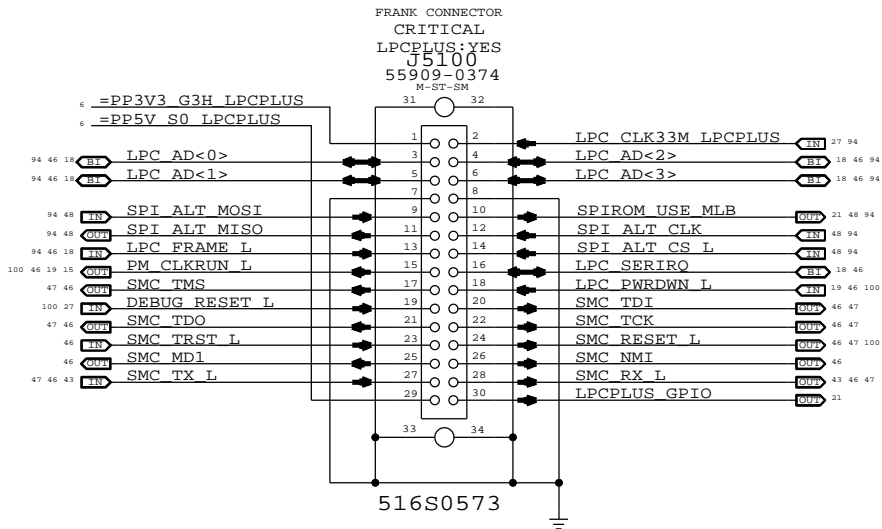
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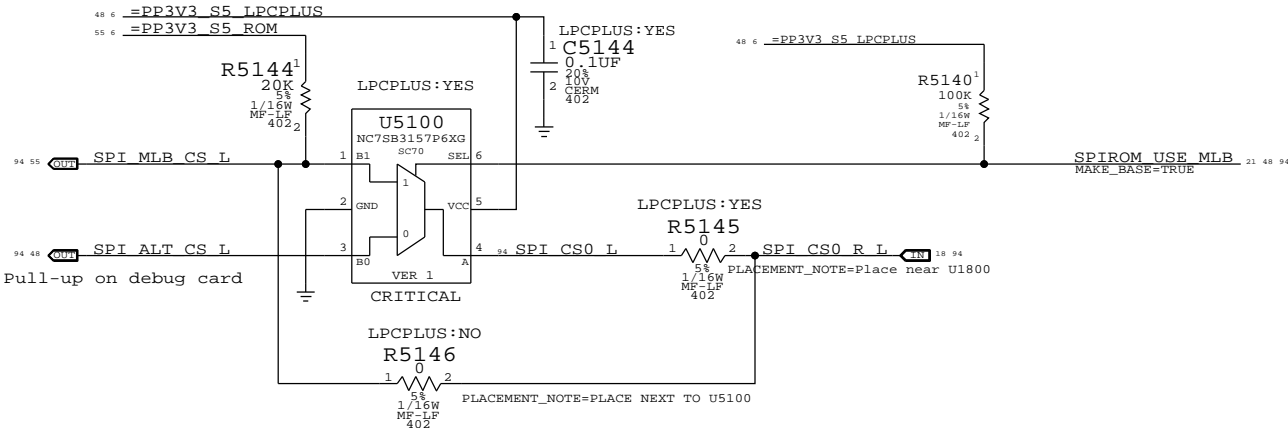
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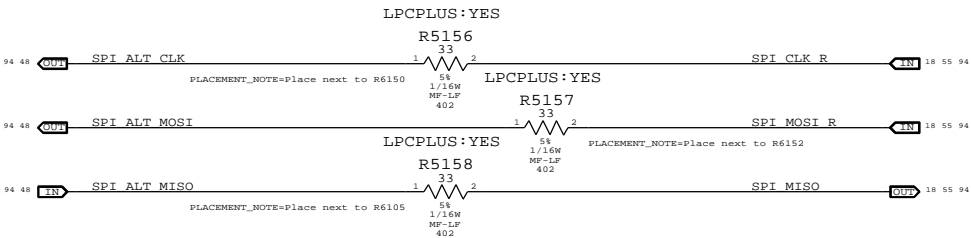
LPC+SPI Connector




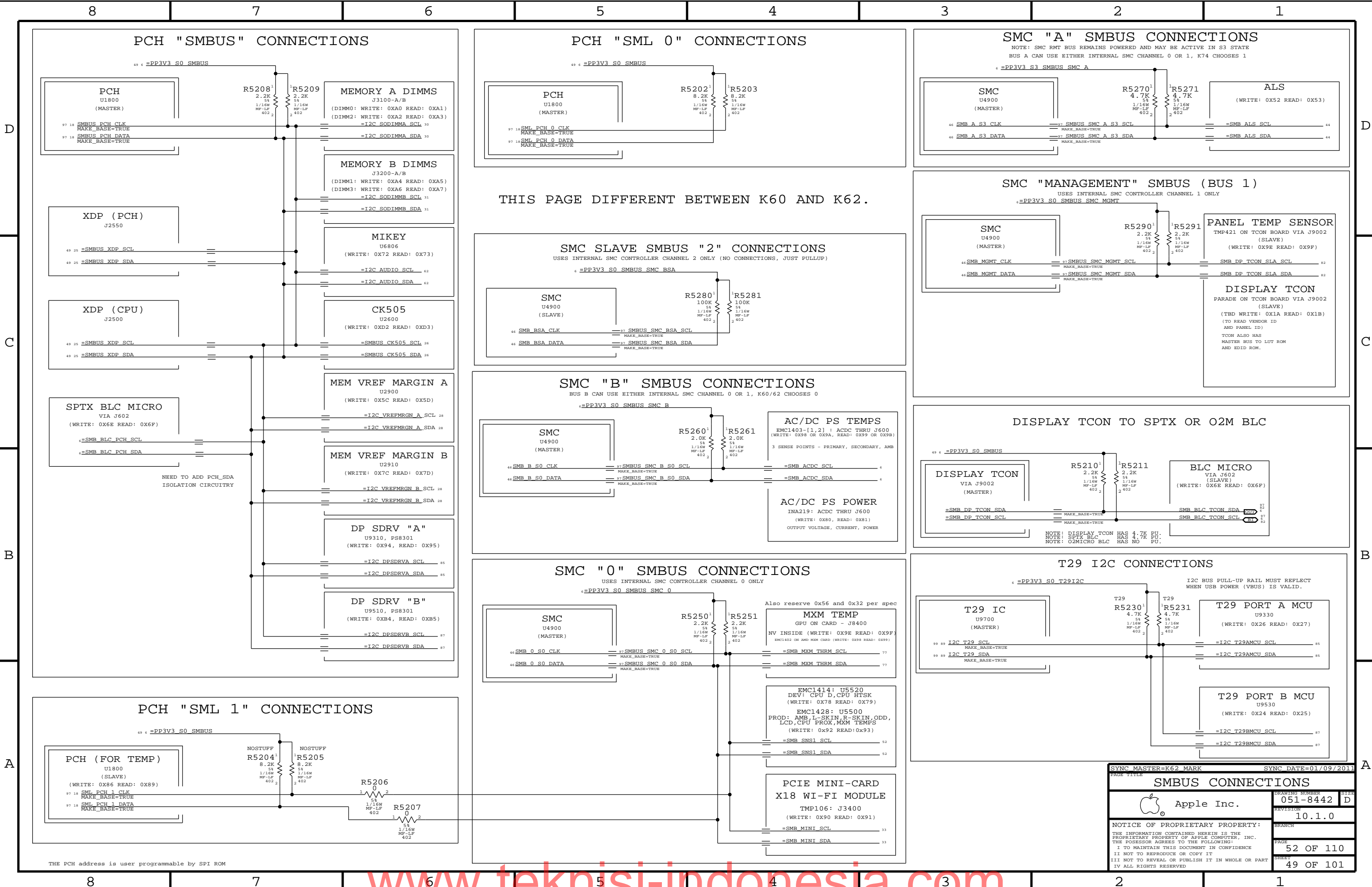
Alternate SPI ROM Support

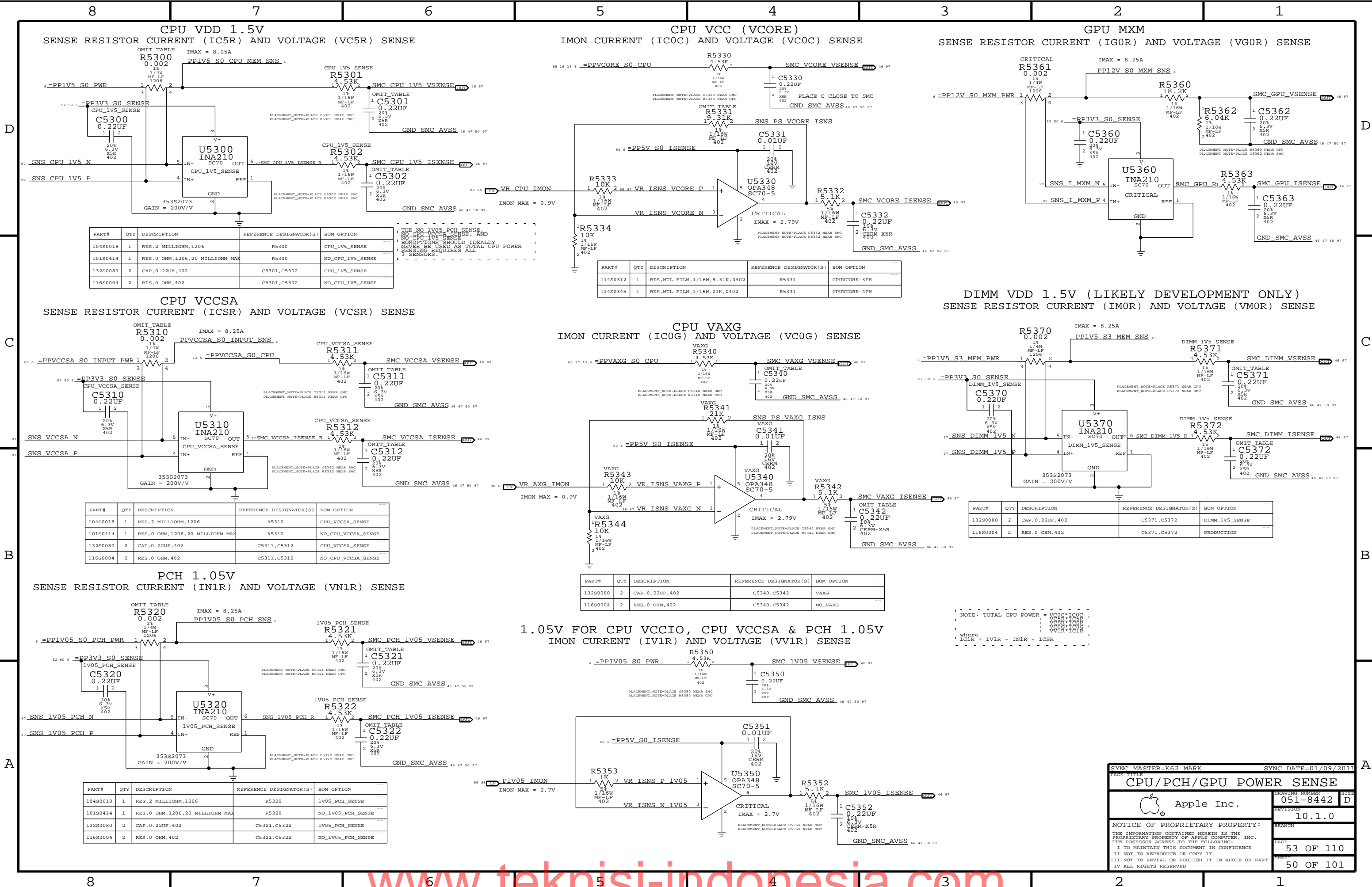


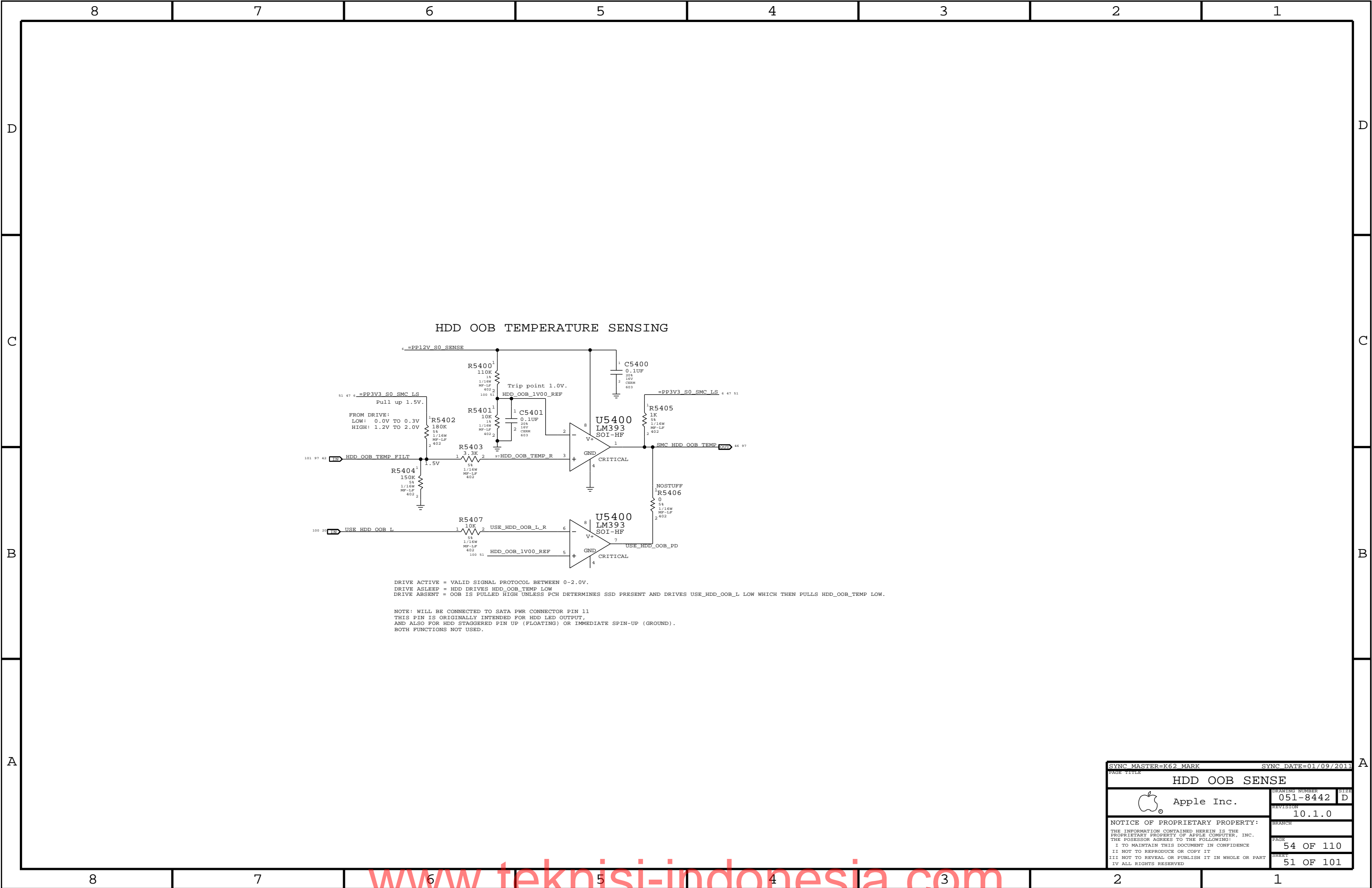
SPI Bus Series Resistance Option



| | | | |
|---|--|----------------------|-----------|
| SYNC MASTER=K62 AARON | | SYNC DATE=11/30/2009 | |
| PAGE TITLE | | | |
| LPC+SPI Debug Connector | | | |
|  Apple Inc. | | DRAWING NUMBER | 051-8442 |
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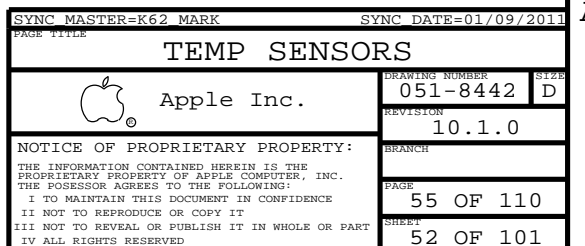
D

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SILK_PART=CPU HSK



D

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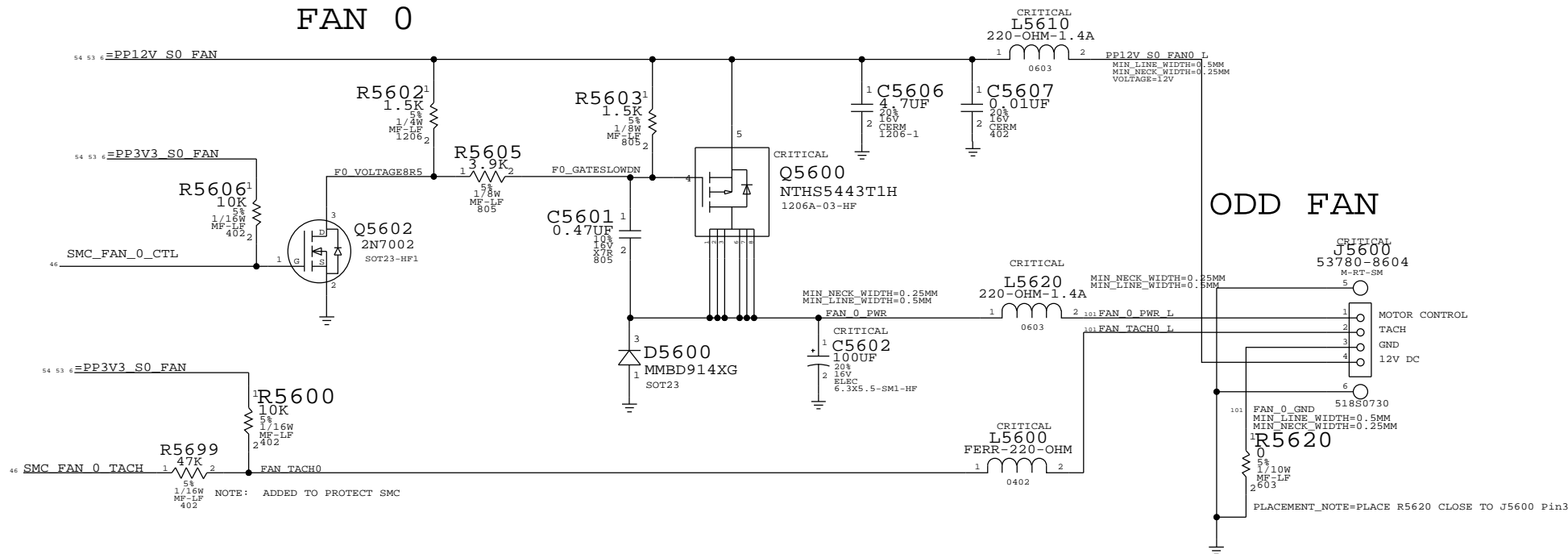
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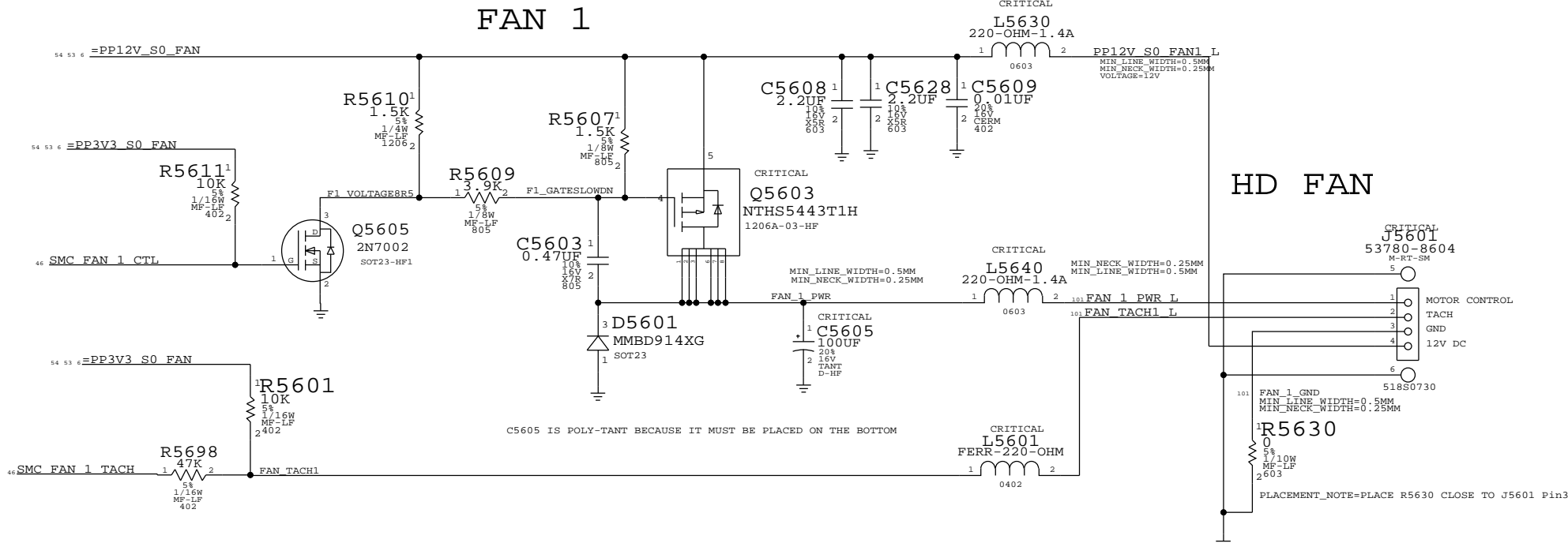
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FAN 0




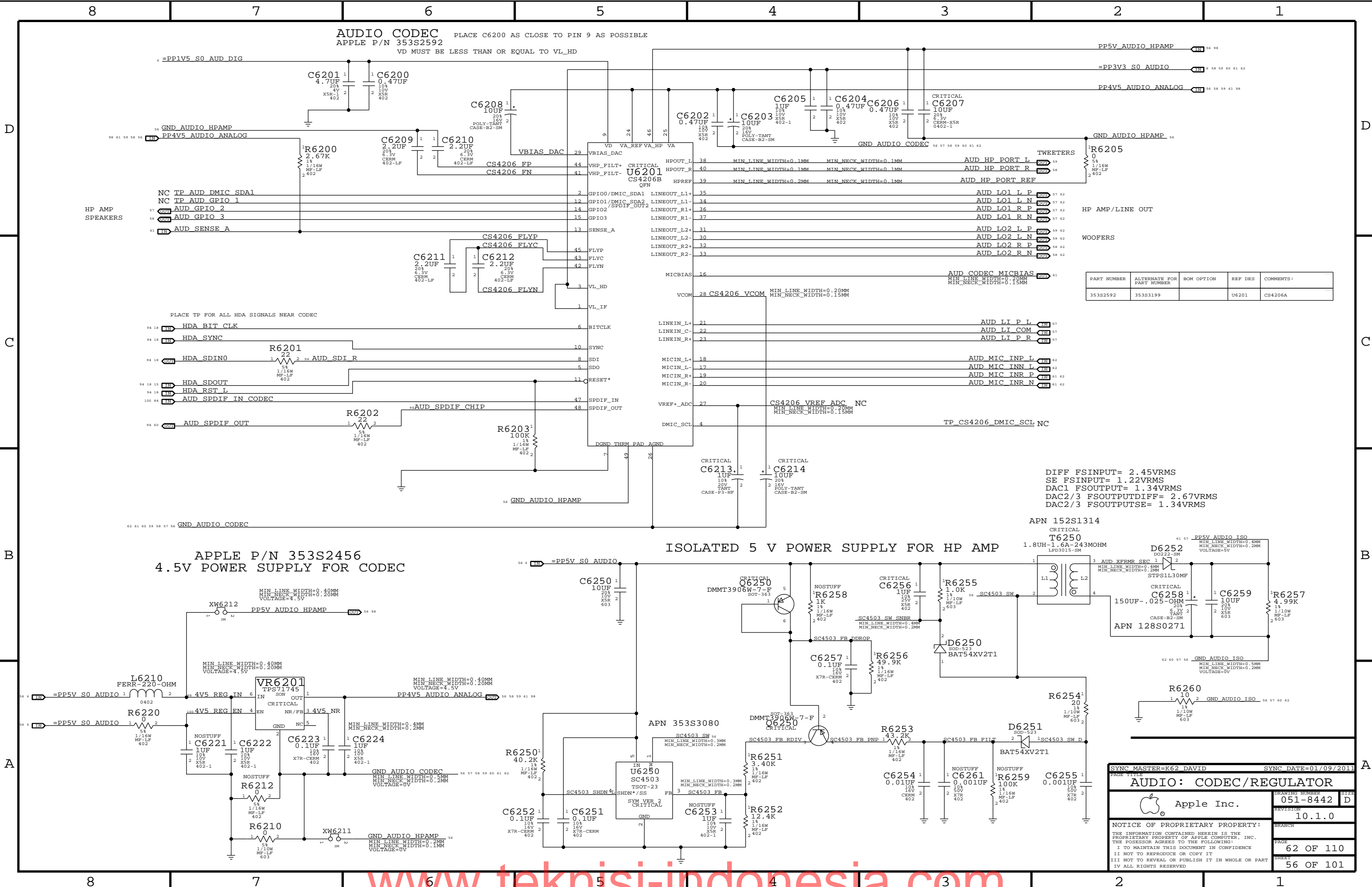
FAN 1



| | | | |
|---|--|----------------------|-----------|
| SYNC MASTER=K62 JERRY | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| HD AND OD FAN | | | |
|  Apple Inc. | | DRAWING NUMBER | 051-8442 |
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|---|--|----------------------|------|
| SYNC MASTER=K62 AARON | | SYNC DATE=11/30/2009 | |
| PAGE TITLE | | | |
| SPI ROM | | | |
|  Apple Inc. | | DRAWING NUMBER | SIZE |
| | | 051-8442 | D |
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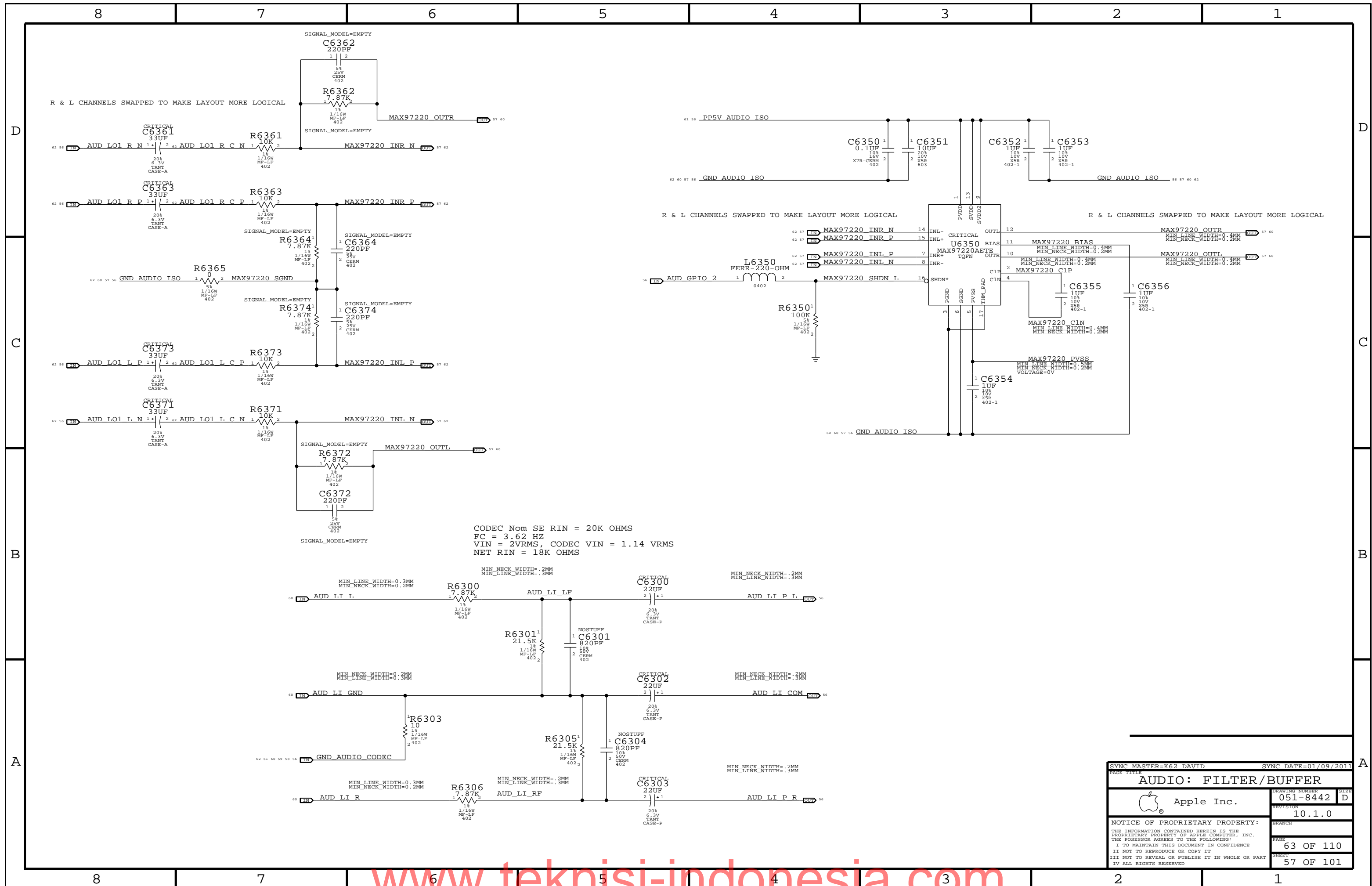
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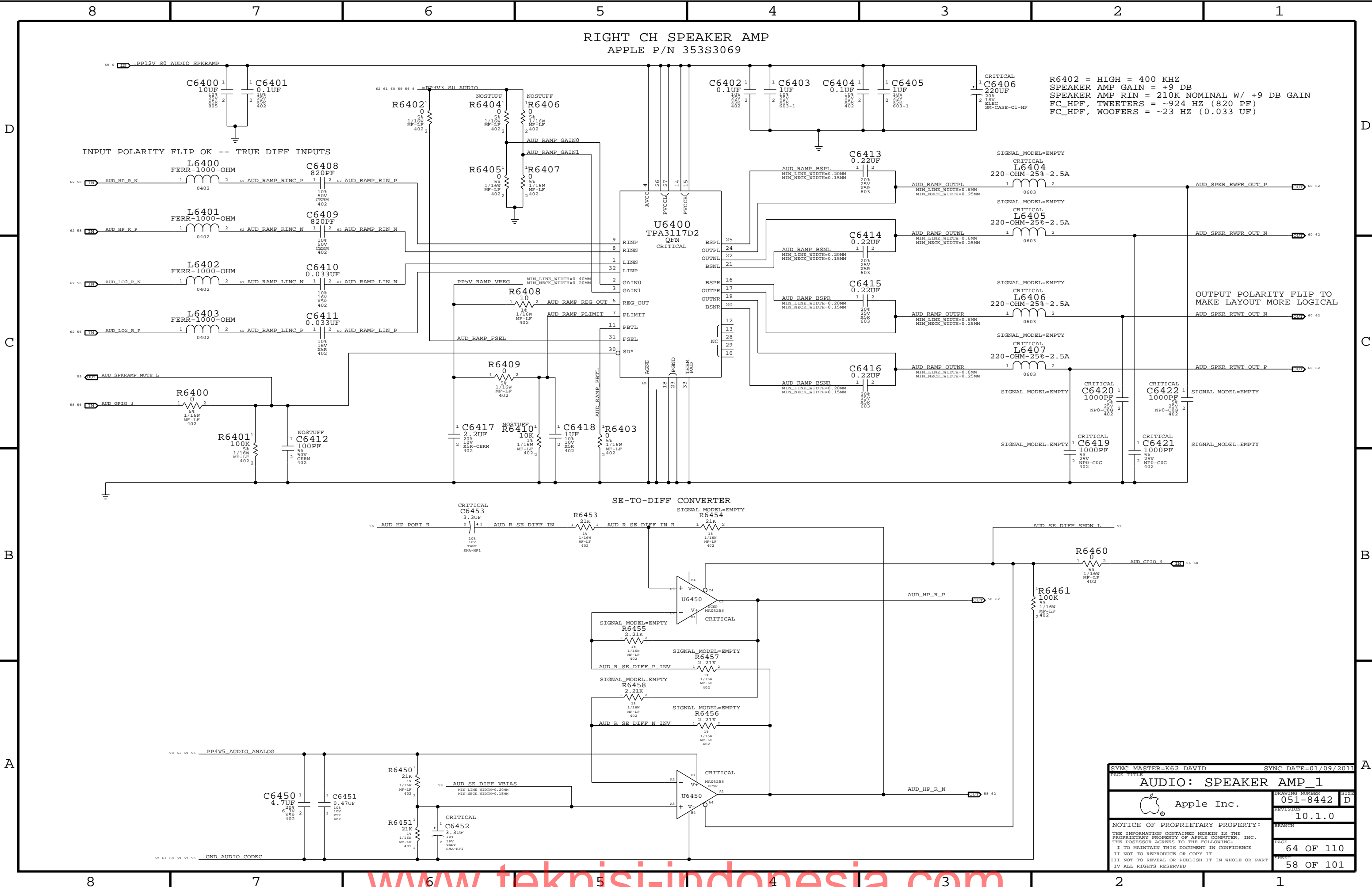
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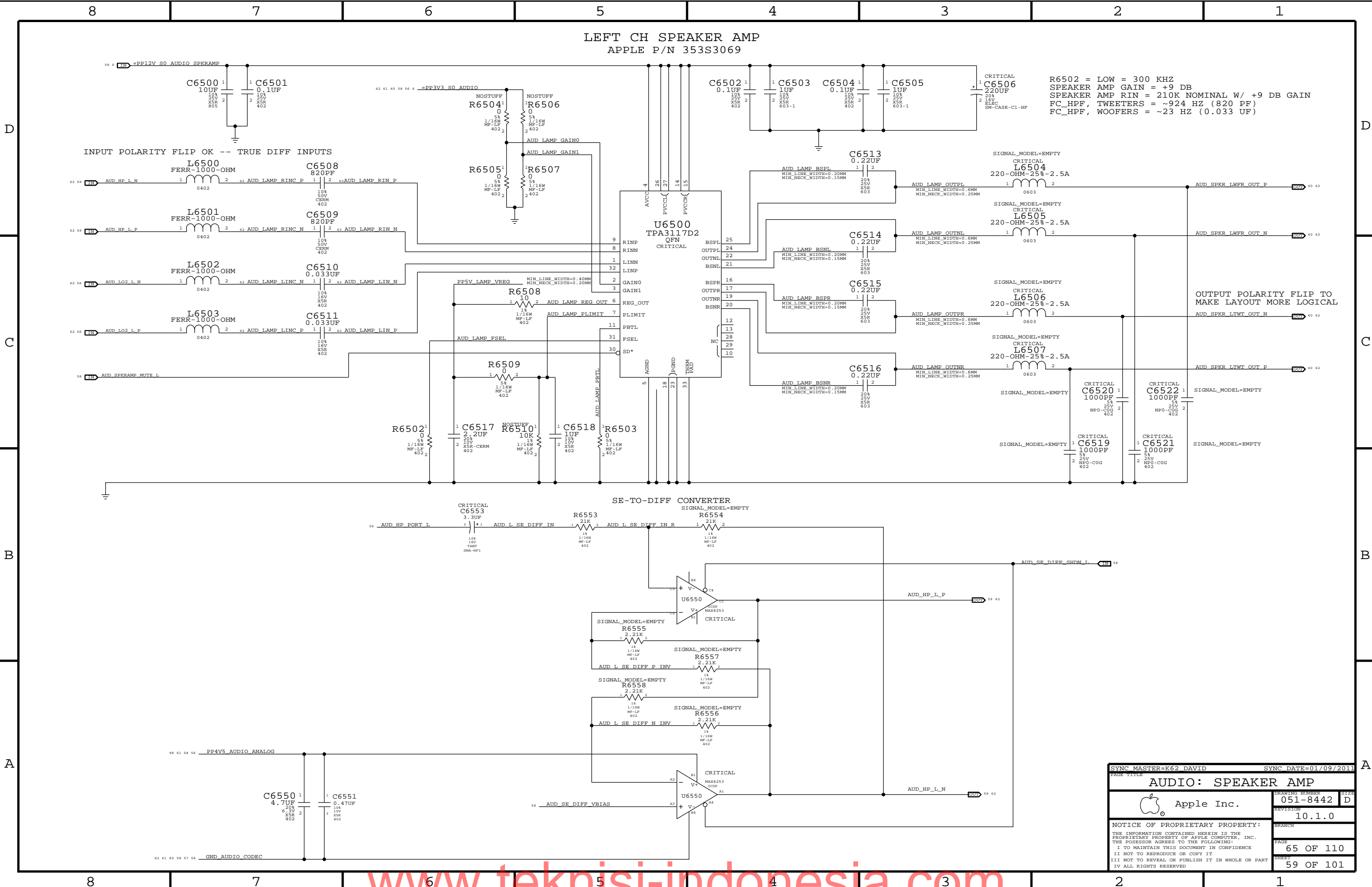
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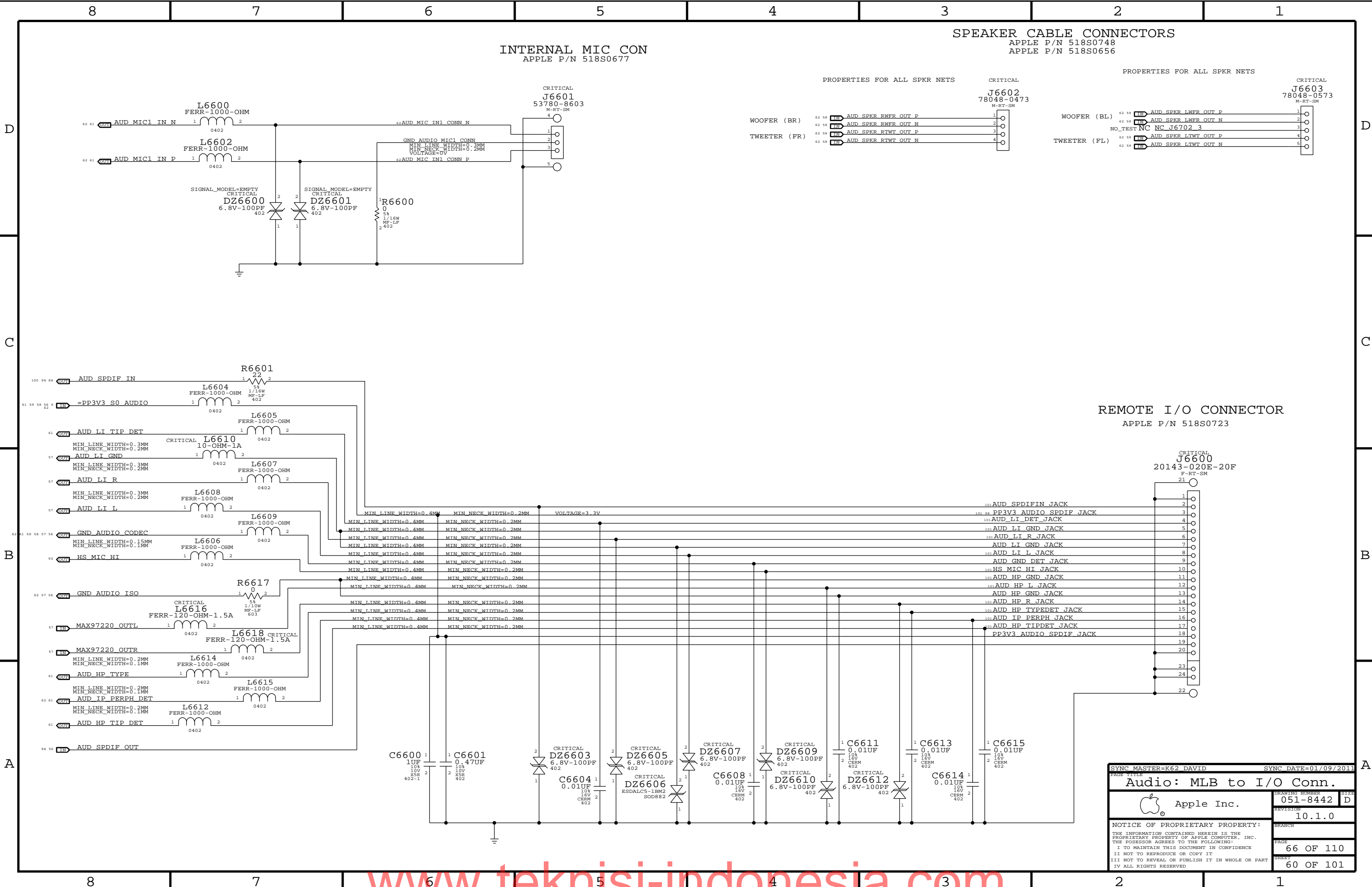
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| SYNC MASTER=K62 DAVID | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| AUDIO: FILTER/BUFFER | | | |
|  Apple Inc. | DRAWING NUMBER | 051-8442 | SIZE |
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| PAGE TITLE | | PAGE NUMBER | |
| AUDIO: SPEAKER AMP_1 | | 051-8442 | |
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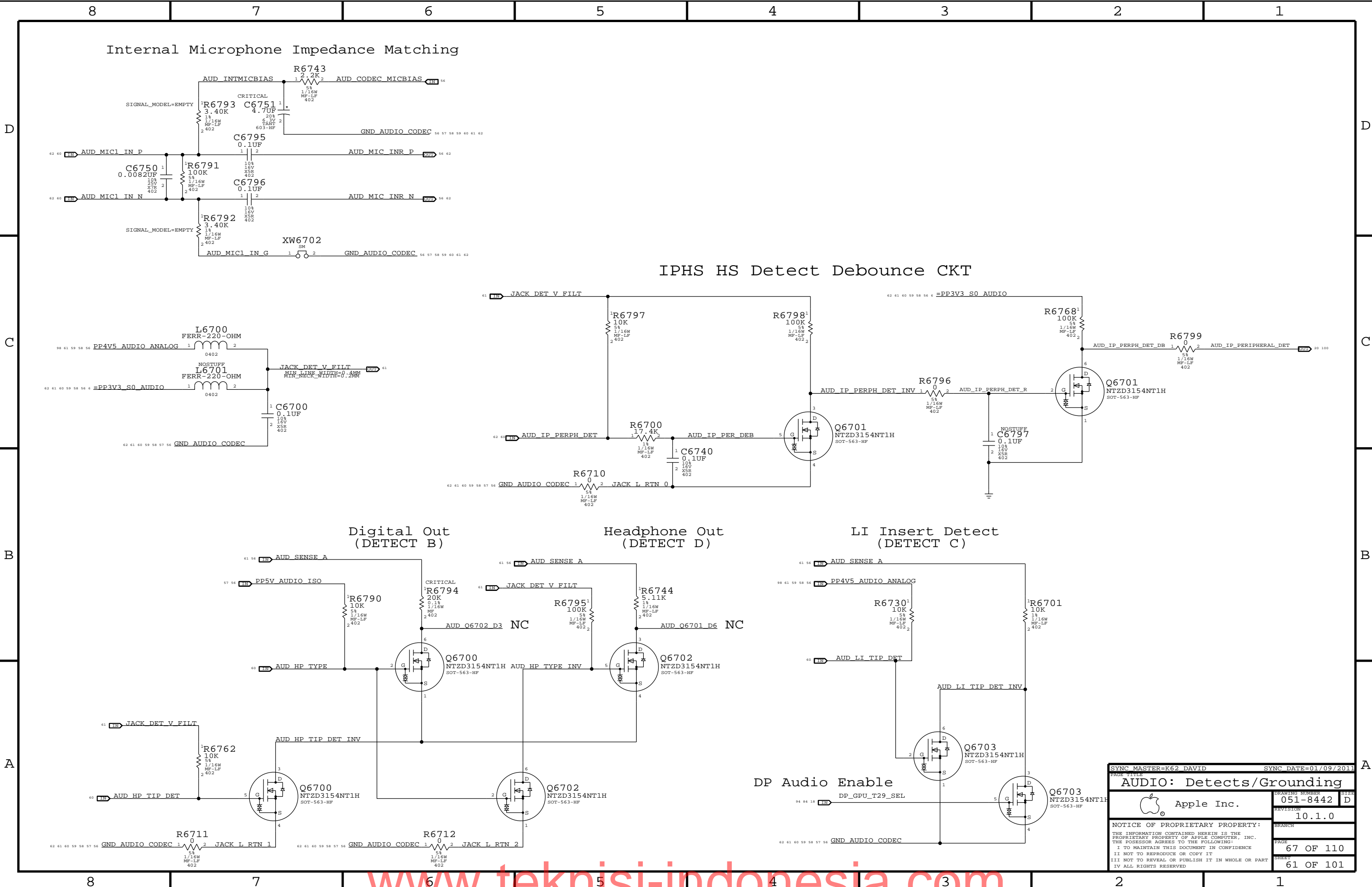
INTERNAL MIC CON
APPLE P/N 518S0677


SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

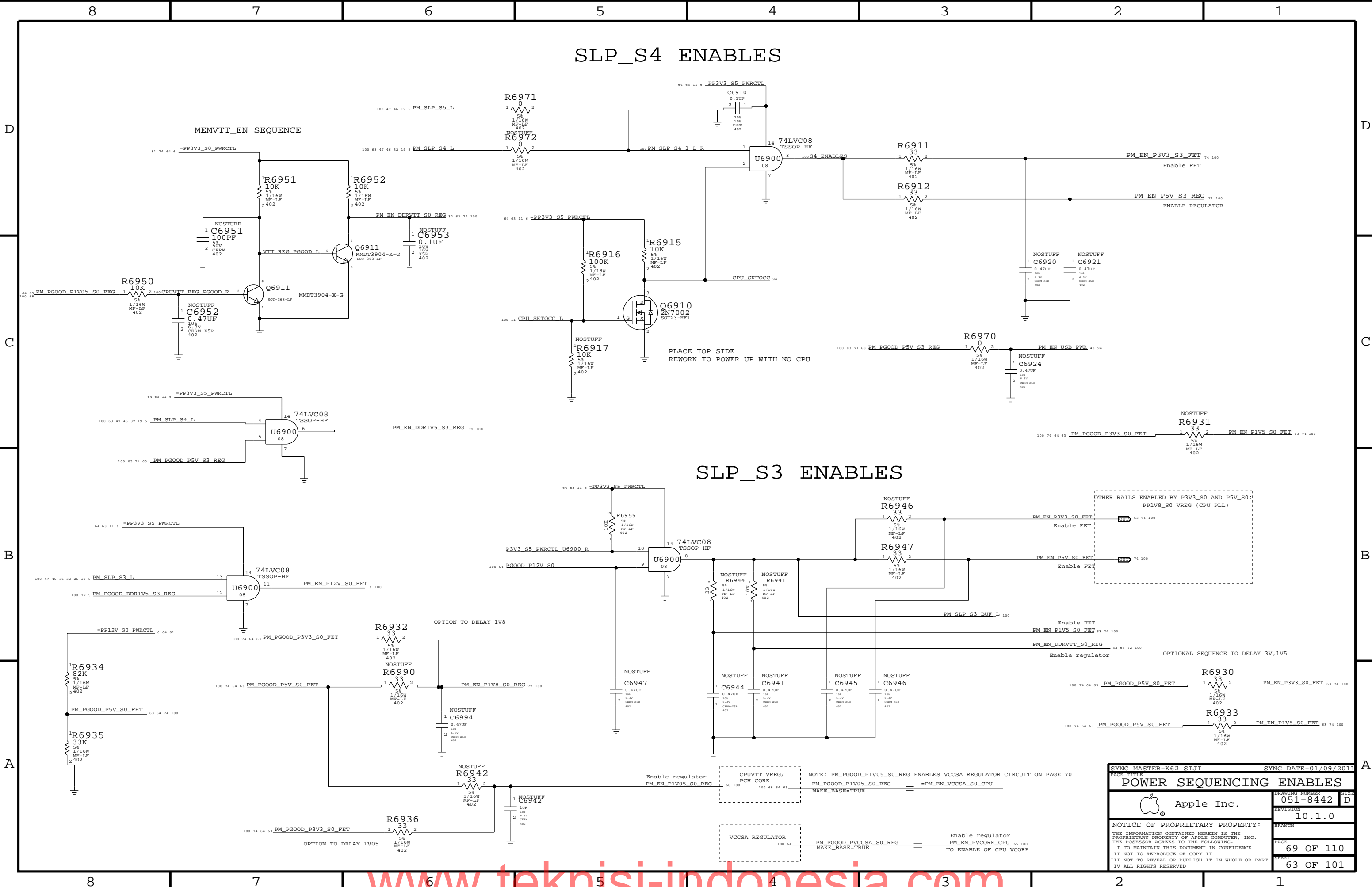
| PROPERTIES FOR ALL SPKR NETS | | CRITICAL | | PROPERTIES FOR ALL SPKR NETS | | CRITICAL | |
|------------------------------|---------------------|----------|------------|------------------------------|---------------------|----------|------------|
| | | J6602 | 78048-0473 | | | J6603 | 78048-0573 |
| | | M-RT-SM | | | | M-RT-SM | |
| WOOFER (BR) | AUD_SPKR_RWER_OUT_P | 1 | | WOOFER (BL) | AUD_SPKR_LWFR_OUT_P | 1 | |
| | AUD_SPKR_RWER_OUT_N | 2 | | | AUD_SPKR_LWFR_OUT_N | 2 | |
| TWEETER (FR) | AUD_SPKR_RTWT_OUT_P | 3 | | NO_TEST | NC_NC_J6702_3 | 3 | |
| | AUD_SPKR_RTWT_OUT_N | 4 | | TWEETER (FL) | AUD_SPKR_LTWT_OUT_P | 4 | |
| | | | | | AUD_SPKR_LTWT_OUT_N | 5 | |


REMOTE I/O CONNECTOR
APPLE P/N 518S0723

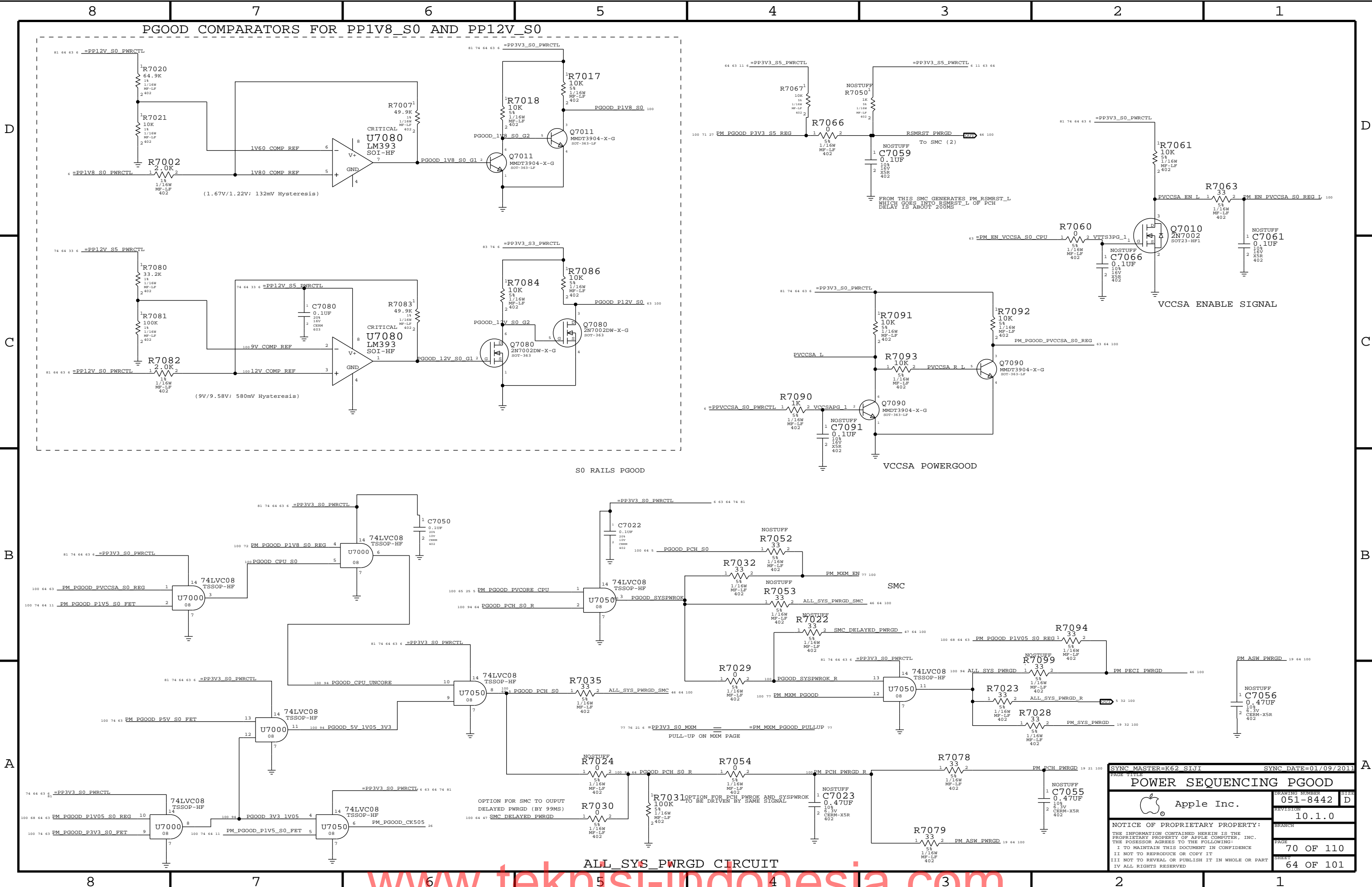
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| Audio: MLB to I/O Conn. | | Drawing Number | |
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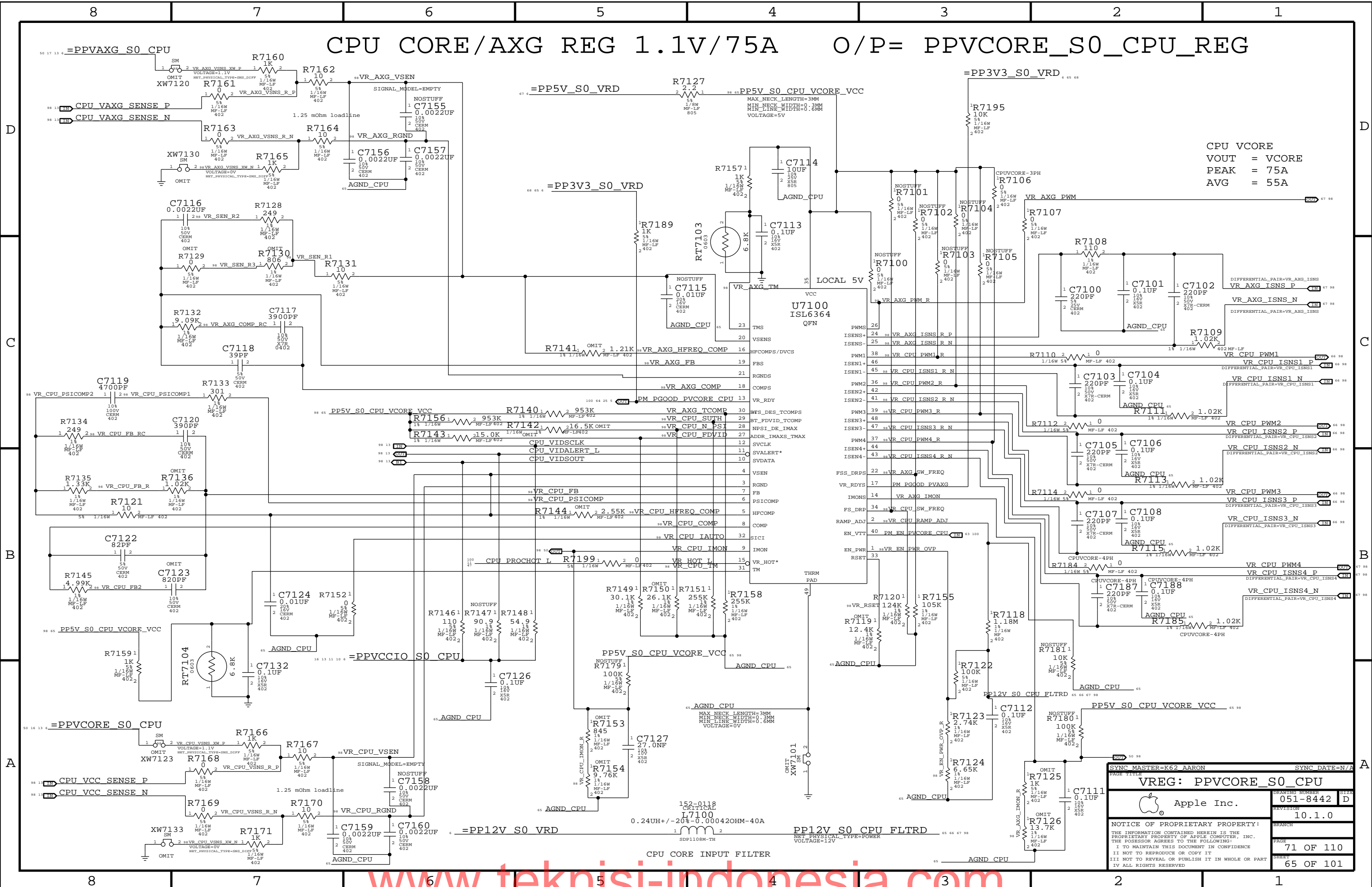


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|---|----------------|----------------------|-----------|
| SYNC MASTER=K62 DAVID | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| AUDIO: Detects/Grounding | | | |
|  | DRAWING NUMBER | | 8442 |
| | 051-8442 | | D |
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|---|--|----------------------|-----------|
| SYNC MASTER=K62 SIJI | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| POWER SEQUENCING | | ENABLES | |
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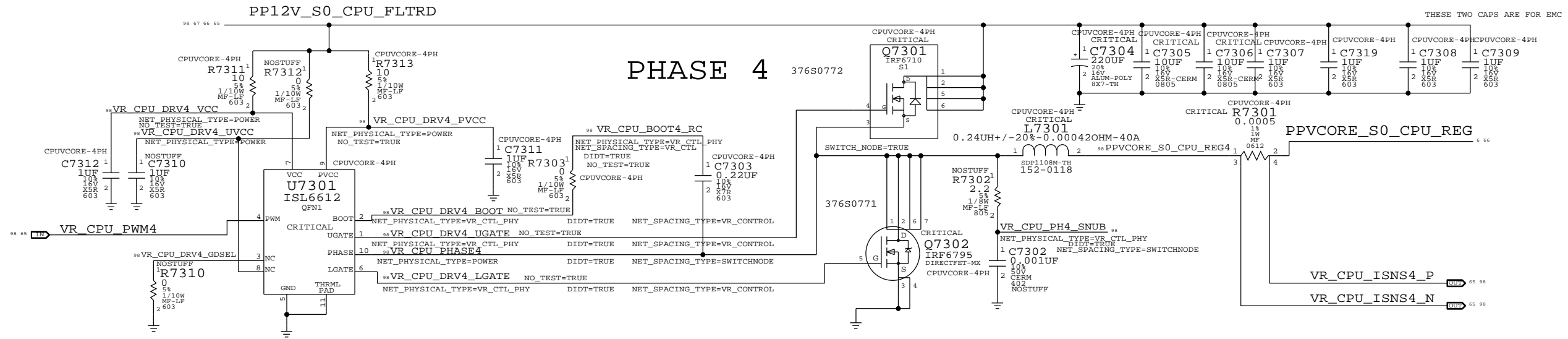


CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG

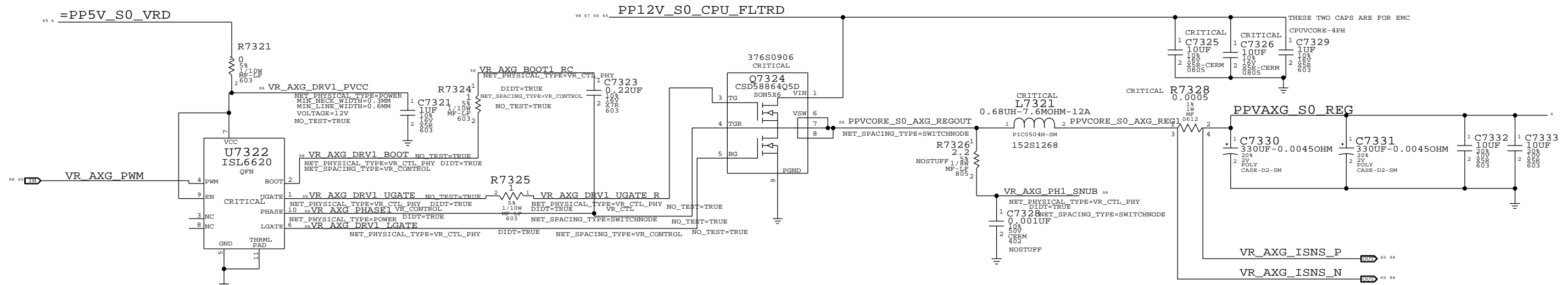
CPU Vcore
VOUT = Vcore
PEAK = 75A
AVG = 55A


| | | | |
|---|--|----------------|--|
| SYNC MASTER=K62 AARON | | SYNC DATE=N/A | |
| PAGE TITLE | | DRAWING NUMBER | |
| VREG: PPVCORE_S0_CPU | | 051-8442 | |
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| THE INFORMATION CONTAINED HEREIN IS THE | | 65 OF 101 | |





AXG PHASE (MAX 15A)



| | | | |
|---|----------------|---------------|------|
| SYNC MASTER=K62 AARON | | SYNC DATE=N/A | |
| PAGE TITLE | | | |
| VREG:AXG PHASE/CORE - CAPS | | | |
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1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG

8

7

6

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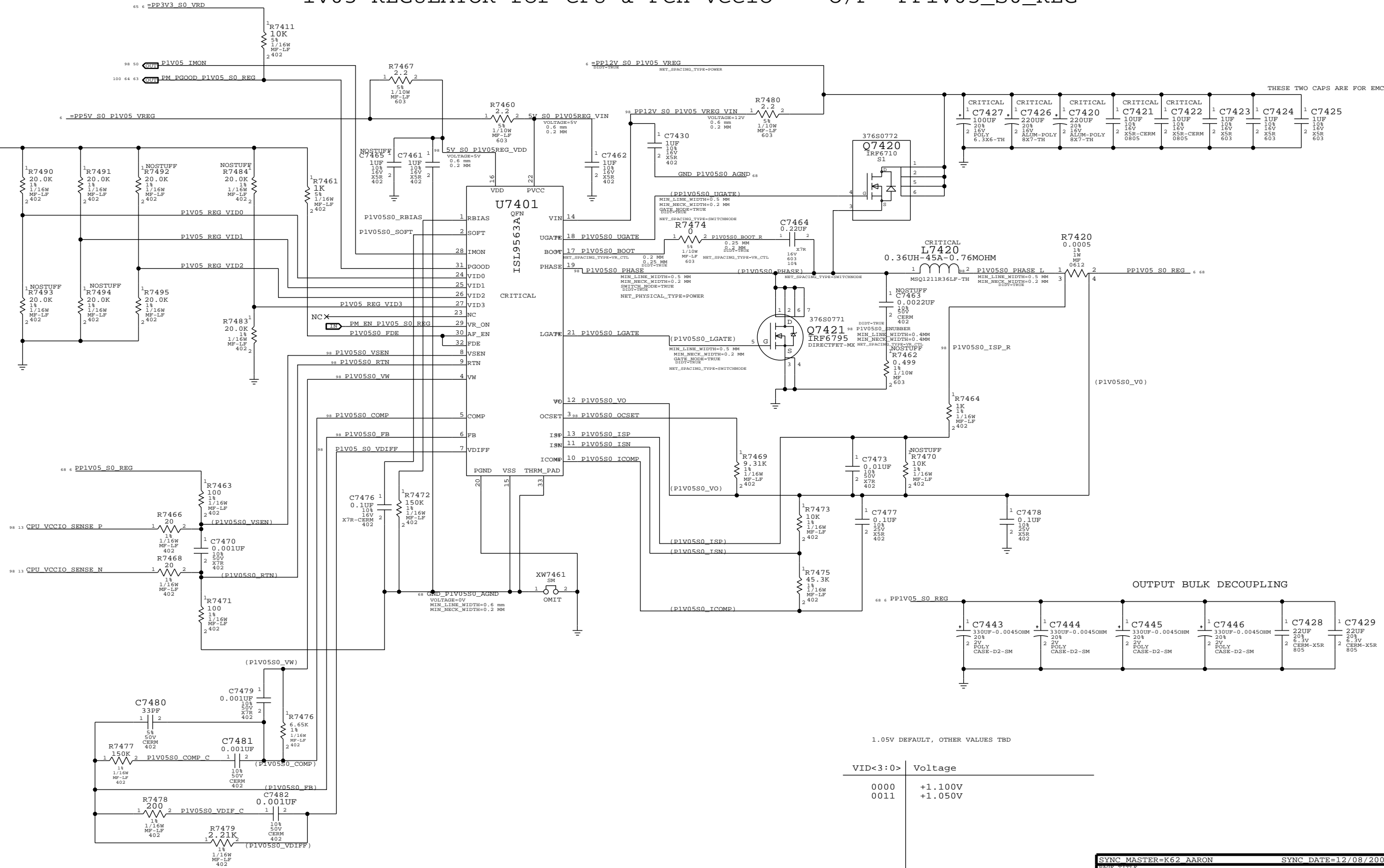
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1.05V DEFAULT, OTHER VALUES TBD

| VID<3:0> | Voltage |
|----------|---------|
| 0000 | +1.100V |
| 0011 | +1.050V |

SYNC MASTER=K62_AARON

SYNC DATE=12/08/2009

1V05 REGULATOR

Apple Inc.

051-8442

10.1.0

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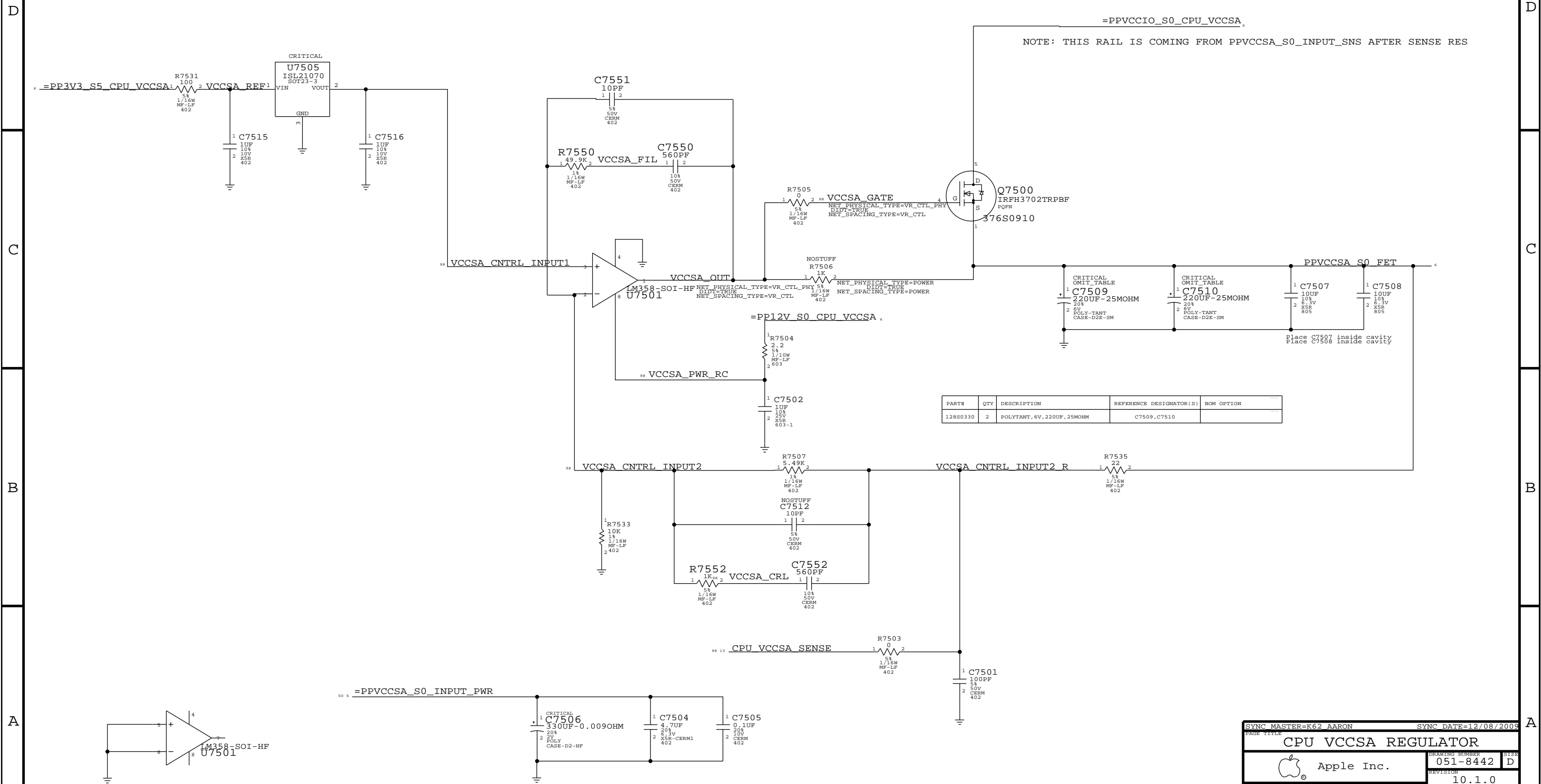
4


3

2

1

CPU VCCSA 0.925V (8.8A MAX)



| | | | |
|---|--|----------------------|--|
| SYNC MASTER=K62 AARON | | SYNC DATE=12/08/2009 | |
| PAGE TITLE | | | |
| CPU VCCSA REGULATOR | | | |
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CPU VCORE 3 PHASE/4 PHASE BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|-----------------------|-------------------------|--------------|
| 116S0066 | 1 | RES,1K,5%,0402 | R7125 | CPUVCORE-4PH |
| 114S0303 | 1 | RES,7.5K,5%,0402 | R7125 | CPUVCORE-3PH |
| 114S0327 | 1 | RES,13.7K,1%,0402 | R7126 | CPUVCORE-4PH |
| 114S0316 | 1 | RES,10.2K,1%,0402 | R7126 | CPUVCORE-3PH |
| 114S0323 | 1 | RES,12.4K,1%,0402 | R7119 | CPUVCORE-4PH |
| 114S0316 | 1 | RES,10.2K,1%,0402 | R7119 | CPUVCORE-3PH |
| 114S0355 | 1 | RES,26.1K,1%,0402 | R7150 | CPUVCORE-4PH |
| 114S0338 | 1 | RES,17.8K,1%,0402 | R7150 | CPUVCORE-3PH |
| 114S0211 | 1 | RES,845,1%,0402 | R7153 | CPUVCORE-4PH |
| 116S0004 | 1 | RES,0,1%,0402 | R7153 | CPUVCORE-3PH |
| 114S0314 | 1 | RES,9.76K,1%,0402 | R7154 | CPUVCORE-4PH |
| 114S0316 | 1 | RES,10.2K,1%,0402 | R7154 | CPUVCORE-3PH |
| 114S0225 | 1 | RES,1.21K,1%,0402 | R7141 | CPUVCORE-4PH |
| 114S0217 | 1 | RES,976,1%,0402 | R7141 | CPUVCORE-3PH |
| 114S0335 | 1 | RES,16.5K,1%,0402 | R7142 | CPUVCORE-4PH |
| 114S0349 | 1 | RES,23.2K,1%,0402 | R7142 | CPUVCORE-3PH |
| 114S0331 | 1 | RES,15K,1%,0402 | R7143 | CPUVCORE-3PH |
| 114S0257 | 1 | RES,2.55K,1%,0402 | R7144 | CPUVCORE-4PH |
| 114S0252 | 1 | RES,2.32K,1%,0402 | R7144 | CPUVCORE-3PH |
| 114S0209 | 1 | RES,806,1%,0402 | R7130 | CPUVCORE-4PH |
| 114S0188 | 1 | RES,487,1%,0402 | R7130 | CPUVCORE-3PH |
| 116S0004 | 1 | RES,0R,1%,0402 | R7129 | CPUVCORE-4PH |
| 114S0189 | 1 | RES,499,1%,0402 | R7129 | CPUVCORE-3PH |
| 114S0219 | 1 | RES,1.02K,1%,0402 | R7136 | CPUVCORE-4PH |
| 114S0131 | 1 | RES,130,1%,0402 | R7136 | CPUVCORE-3PH |
| 132S8221 | 1 | CAP,820PF,10%,0402 | C7123 | CPUVCORE-4PH |
| 132S1534 | 1 | CAP,0.0012UF,10%,0402 | C7123 | CPUVCORE-3PH |

SYNC MASTER=K62_AARON

SYNC DATE=12/08/2009

CPU 3P/4P BOM OPTIONS

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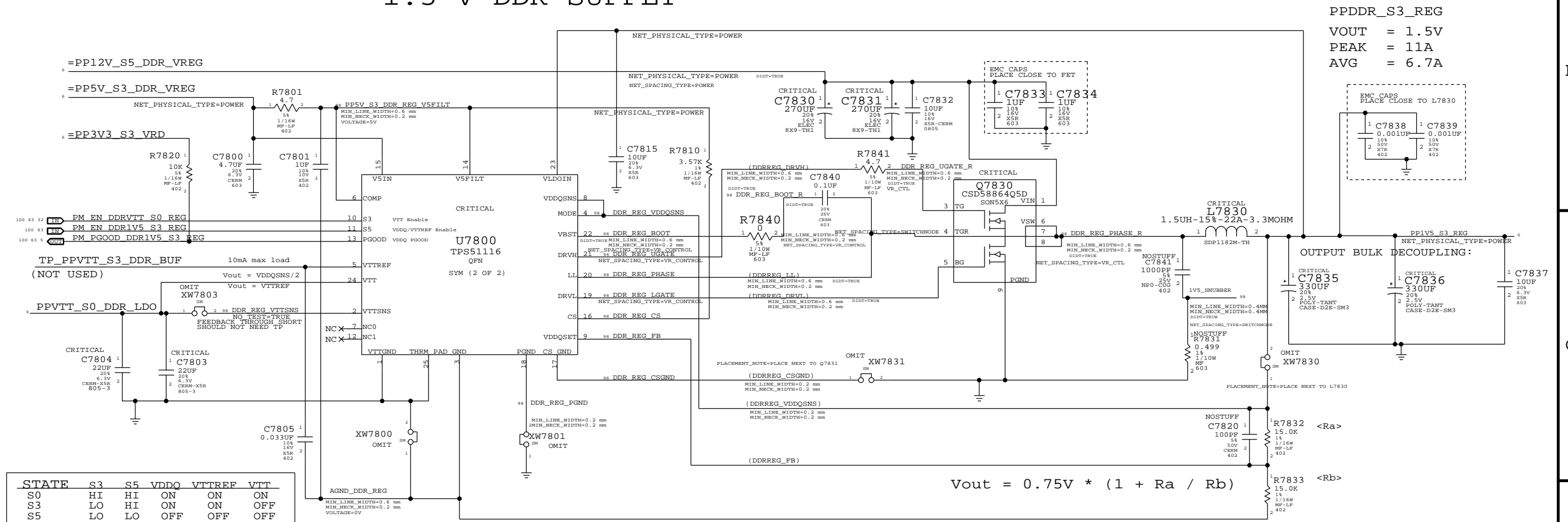
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1.5 V DDR SUPPLY

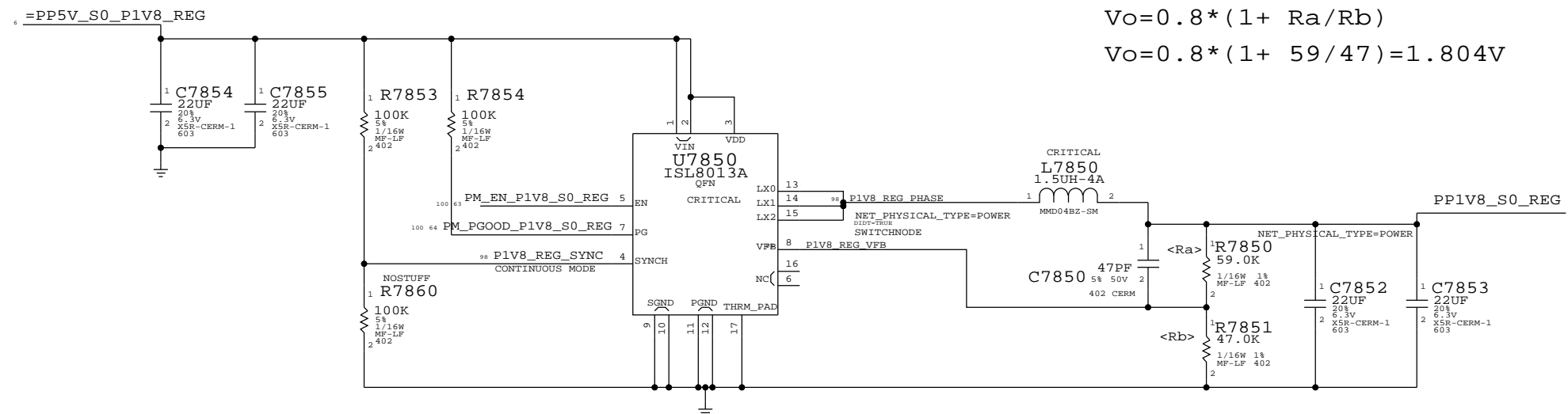


1.8 V SUPPLY


1A Average current

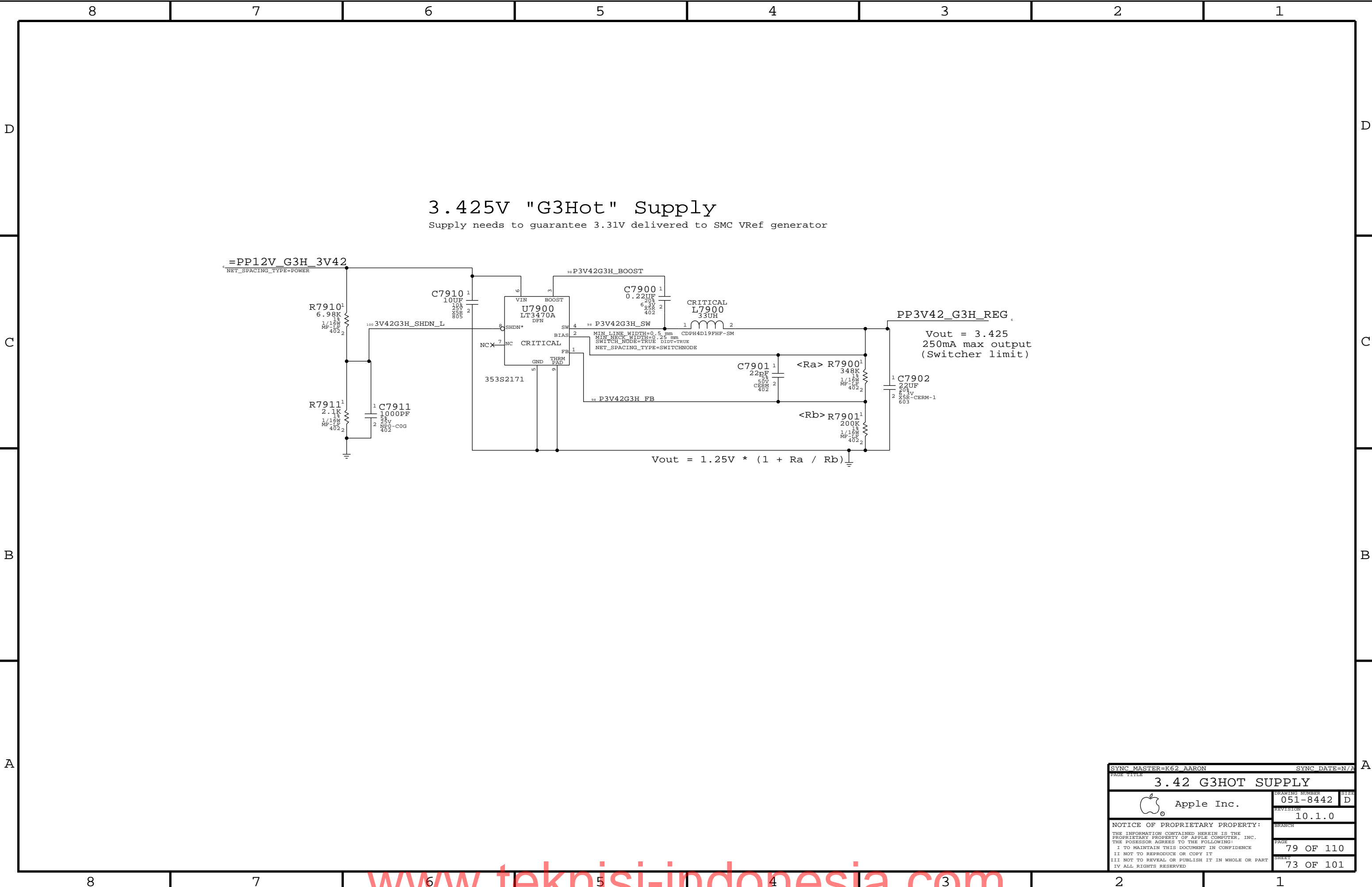
$$V_o = 0.8 * (1 + R_a / R_b)$$


$$V_o = 0.8 * (1 + 59 / 47) = 1.804V$$

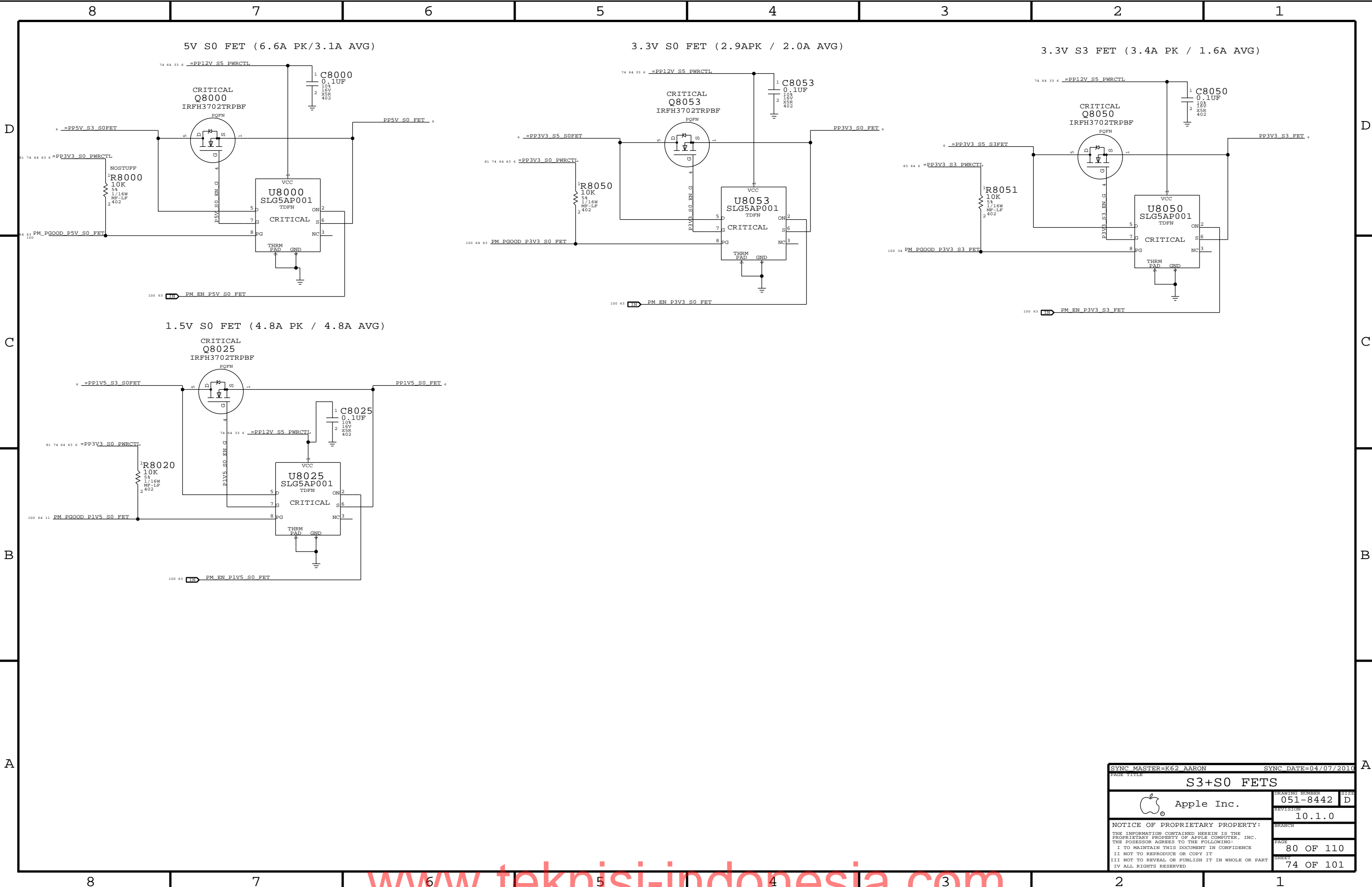


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| PAGE TITLE | | | |
| 1.5V / 1.8V VREGS | | | |
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| PAGE TITLE | | | |
| 3.42 G3HOT SUPPLY | | | |
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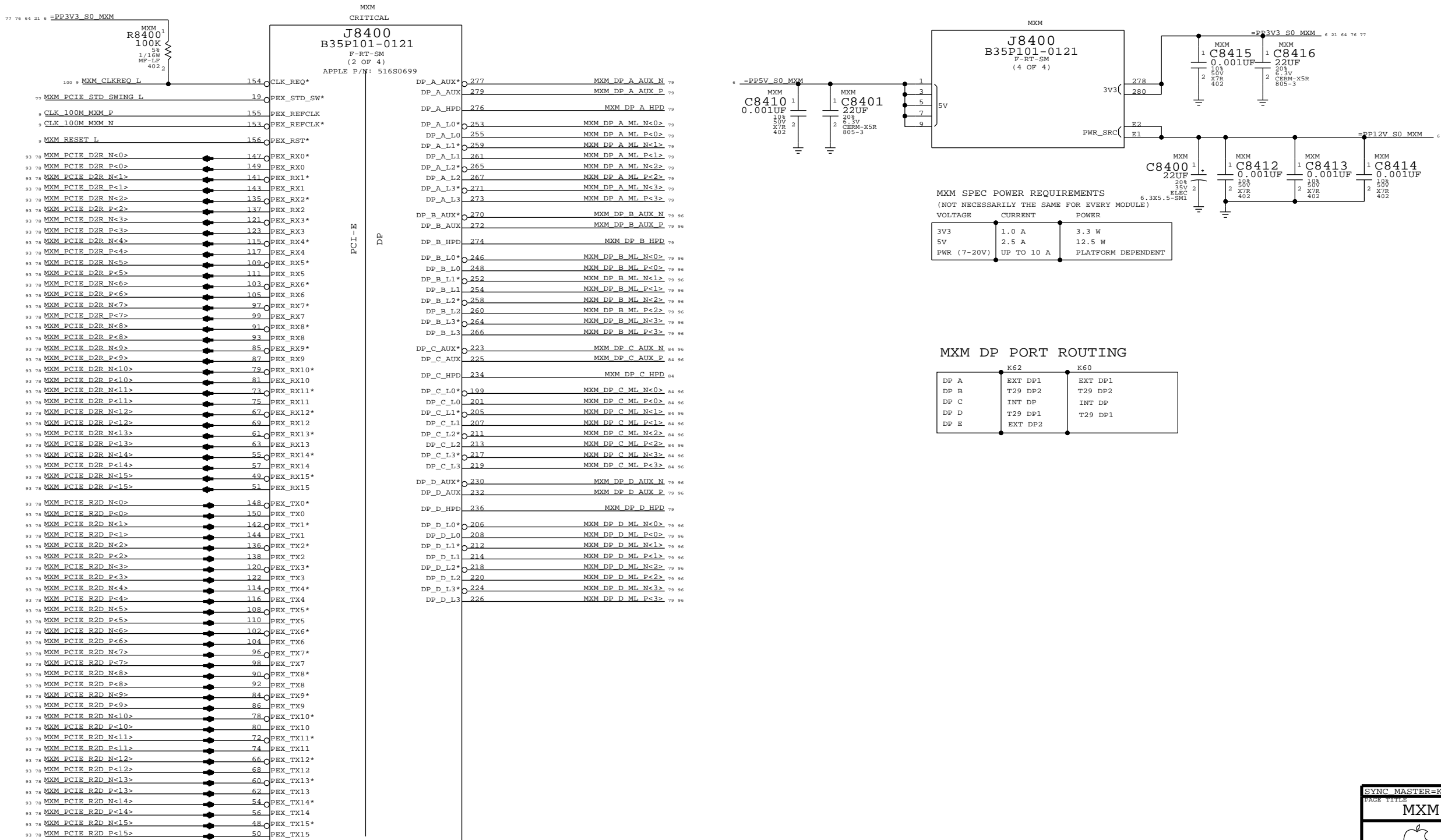



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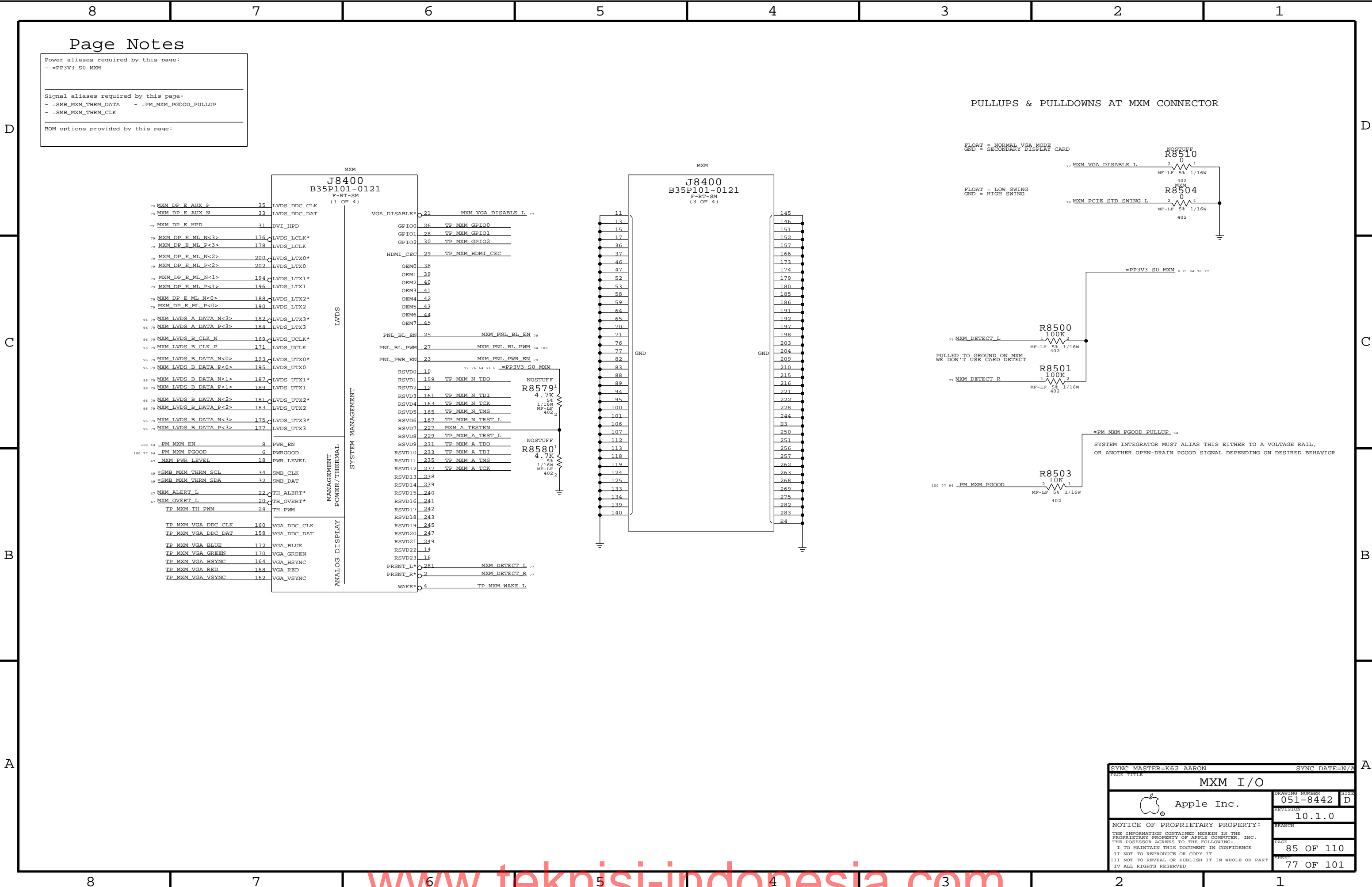
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- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



| | | | |
|---|--|----------------|----------|
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| PAGE TITLE | | | |
| MXM PCIe, DP & Power | | | |
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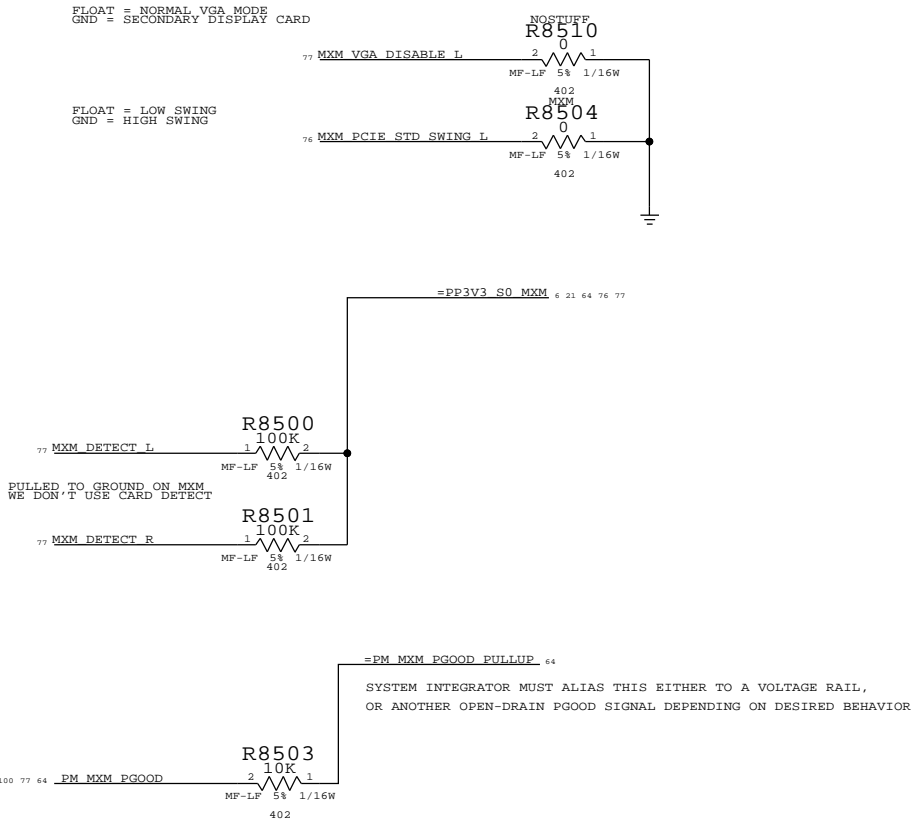
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Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



| | | | |
|---|--|----------------|-----------|
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| PAGE TITLE | | | |
| MXM I/O | | | |
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| | | | | | | | |
|-------------|-------|-----|--------------------|-------------------|-------------------|--------------------|----------|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| MXM TX CAPS | | | | MXM RX CAPS | | | |
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| MXM TX CAPS | | | | MXM RX CAPS | | | |
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

SYNC MASTER=K62

SYNC DATE=N/A

PAGE TITLE

MXM PCIE CAPS

 Apple Inc.

DRAWING NUMBER

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Page Notes

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Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

| | | | | | |
|----|----------------------------------|----|----------------------|----|--------------|
| 76 | <u>MXM DP A ML P<0..3></u> | == | DP_EXTM_ML_C_P<0..3> | 85 | 96 |
| | | | MAKE_BASE=TRUE | | NO_TEST=TRUE |
| 76 | <u>MXM DP A ML N<0..3></u> | == | DP_EXTM_ML_C_N<0..3> | 85 | 96 |
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| 76 | <u>MXM DP A AUX P</u> | | DP_EXTM_AUXCH_C_P | 79 | 85 96 |
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| 76 | <u>MXM DP A AUX N</u> | | DP_EXTM_AUXCH_C_N | 79 | 85 96 |
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| 76 | <u>MXM DP A HPD</u> | | DP_EXTM_HPD | 85 | |
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| 77 | <u>MXM DP E ML P<0..3></u> | == | DP_EXTM_ML_C_P<0..3> | 87 | 96 |
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| 77 | <u>MXM DP E AUX P</u> | | DP_EXTM_AUXCH_C_P | 79 | 87 96 |
| | | | MAKE_BASE=TRUE | | NO_TEST=TRUE |
| 77 | <u>MXM DP E AUX N</u> | | DP_EXTM_AUXCH_C_N | 79 | 87 96 |
| | | | MAKE_BASE=TRUE | | NO_TEST=TRUE |
| 77 | <u>MXM DP E HPD</u> | | DP_EXTM_HPD | 87 | |
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DDC/AUX ALIAS

| | | | | | | |
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| | | | MAKE_BASE=TRUE | | | |
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| 96 | 87 | 79 | DP_EXTB_AUXCH_C_P | == | DP_EXTB_DDC_CLK | 87 |
| | | | MAKE_BASE=TRUE | | | |
| 96 | 87 | 79 | DP_EXTB_AUXCH_C_N | == | DP_EXTB_DDC_DATA | 87 |
| | | | MAKE_BASE=TRUE | | | |

NO_TEST T29 & DP DC BIAS

| | | | | | |
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| 199 | DP A BIAS P 2 | 05 06 | 200 | DP B BIAS P 2 | 07 08 |
| 200 | NO TEST=TRUE | | 201 | NO TEST=TRUE | |
| 201 | DP A BIAS N 2 | 05 06 | 202 | DP B BIAS P 2 | 07 08 |
| 202 | NO TEST=TRUE | | 203 | NO TEST=TRUE | |
| 203 | DP A BIAS P 3 | 05 06 | 204 | DP B BIAS P 3 | 07 08 |
| 204 | NO TEST=TRUE | 05 09 | 205 | NO TEST=TRUE | |

T29 CONN POWER AND CONTROL ALIAS


| | | | | | | | | | |
|-----|---------------------|-----------------------------------|-----------------------|---------------------------------------|-----------------------|-----------------------|---------------------|----|----|
| | <u>6</u> | <u>PP3V3 SW DPAPWR</u> | <u>==</u> | <u>PP3V3 SW DPAPWR</u> | 95 | 98 | | | |
| | <u>6</u> | <u>PP3V3 SW DPBPWR</u> | <u>==</u> | <u>PP3V3 SW DPBPWR</u> | 97 | 98 | | | |
| 100 | 36 | 33 | 19 | <u>PCIE WAKE L</u> | <u>==</u> | <u>T29 WAKE L</u> | 95 | 97 | |
| 96 | 76 | <u>MXM DP B ML P<0...3></u> | <u>==</u> | <u>DP T29SNK1 ML C P<0...3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 96 | 76 | <u>MXM DP B ML N<0...3></u> | <u>==</u> | <u>DP T29SNK1 ML C N<0...3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 96 | 76 | <u>MXM DP B AUX P</u> | <u>==</u> | <u>DP T29SNK1 AUXCH C P</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 96 | 76 | <u>MXM DP B AUX N</u> | <u>==</u> | <u>DP T29SNK1 AUXCH C N</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 76 | <u>MXM DP B HPD</u> | <u>==</u> | <u>DP T29SNK1 HPD</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | | |
| 96 | 76 | <u>MXM DP D ML P<0...3></u> | <u>==</u> | <u>DP T29SNK0 ML C P<0...3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 96 | 76 | <u>MXM DP D ML N<0...3></u> | <u>==</u> | <u>DP T29SNK0 ML C N<0...3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 96 | 76 | <u>MXM DP D AUX P</u> | <u>==</u> | <u>DP T29SNK0 AUXCH C P</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 96 | 76 | <u>MXM DP D AUX N</u> | <u>==</u> | <u>DP T29SNK0 AUXCH C N</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | 99 |
| 76 | <u>MXM DP D HPD</u> | <u>==</u> | <u>DP T29SNK0 HPD</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO_TEST=TRUE</u> | 95 | | |

UNUSED MXM CONTROL SIGNALS

| | | | |
|----|-----------------------|----|-----------------------------|
| 77 | <u>MXM_PNL_BL_EN</u> | == | NC_MXM_PNL_BL_EN |
| | | == | MAKE_BASE=TRUE NO_TEST=TRUE |
| 77 | <u>MXM_PNL_PWR_EN</u> | == | NC_MXM_PNL_PWR_EN |
| | | == | MAKE_BASE=TRUE NO_TEST=TRUE |

Unused MXM Interfaces

| | | | | | | | |
|----|----|-----------------------------------|-----------|--------------------------------------|-----------|-----------------------|---------------------|
| 95 | 77 | <u>MMX LVDS A DATA N<3></u> | <u>==</u> | <u>NC MMX LVDS A DATA N<3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS A DATA P<3></u> | <u>==</u> | <u>NC MMX LVDS A DATA P<3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B CLK N</u> | <u>==</u> | <u>NC MMX LVDS B CLK N</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B CLK P</u> | <u>==</u> | <u>NC MMX LVDS B CLK P</u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA N<0></u> | <u>==</u> | <u>NC MMX LVDS B DATA N<0></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA P<0></u> | <u>==</u> | <u>NC MMX LVDS B DATA P<0></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA N<1></u> | <u>==</u> | <u>NC MMX LVDS B DATA N<1></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA P<1></u> | <u>==</u> | <u>NC MMX LVDS B DATA P<1></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA N<2></u> | <u>==</u> | <u>NC MMX LVDS B DATA N<2></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA P<2></u> | <u>==</u> | <u>NC MMX LVDS B DATA P<2></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA N<3></u> | <u>==</u> | <u>NC MMX LVDS B DATA N<3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |
| 96 | 77 | <u>MMX LVDS B DATA P<3></u> | <u>==</u> | <u>NC MMX LVDS B DATA P<3></u> | <u>==</u> | <u>MAKE_BASE=TRUE</u> | <u>NO TEST=TRUE</u> |

| | | | |
|---|--|----------------|------|
| SYNC MASTER=K62 AARON | | SYNC DATE=N/A | |
| PAGE TITLE | | | |
| DP ALIAS | | | |
|  Apple Inc. | | DRAWING NUMBER | SIZE |
| | | 051-8442 | D |
| | | REVISION | |
| | | 10.1.0 | |
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GreenCLK Implementation Notes:

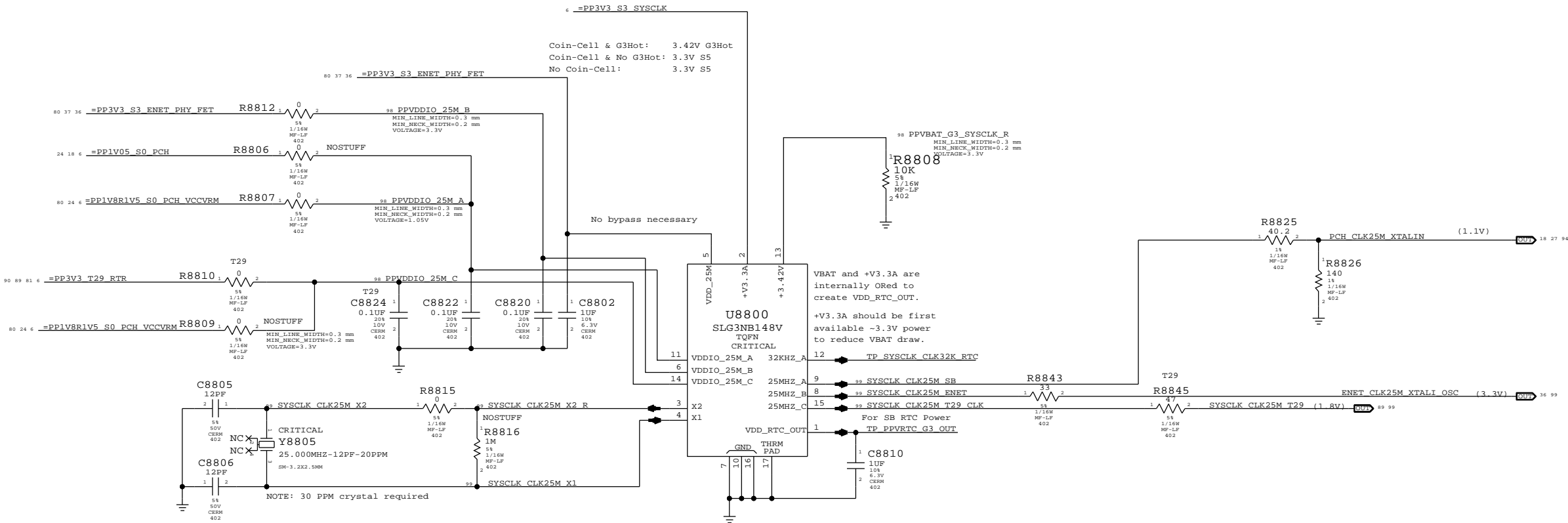
VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)


VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

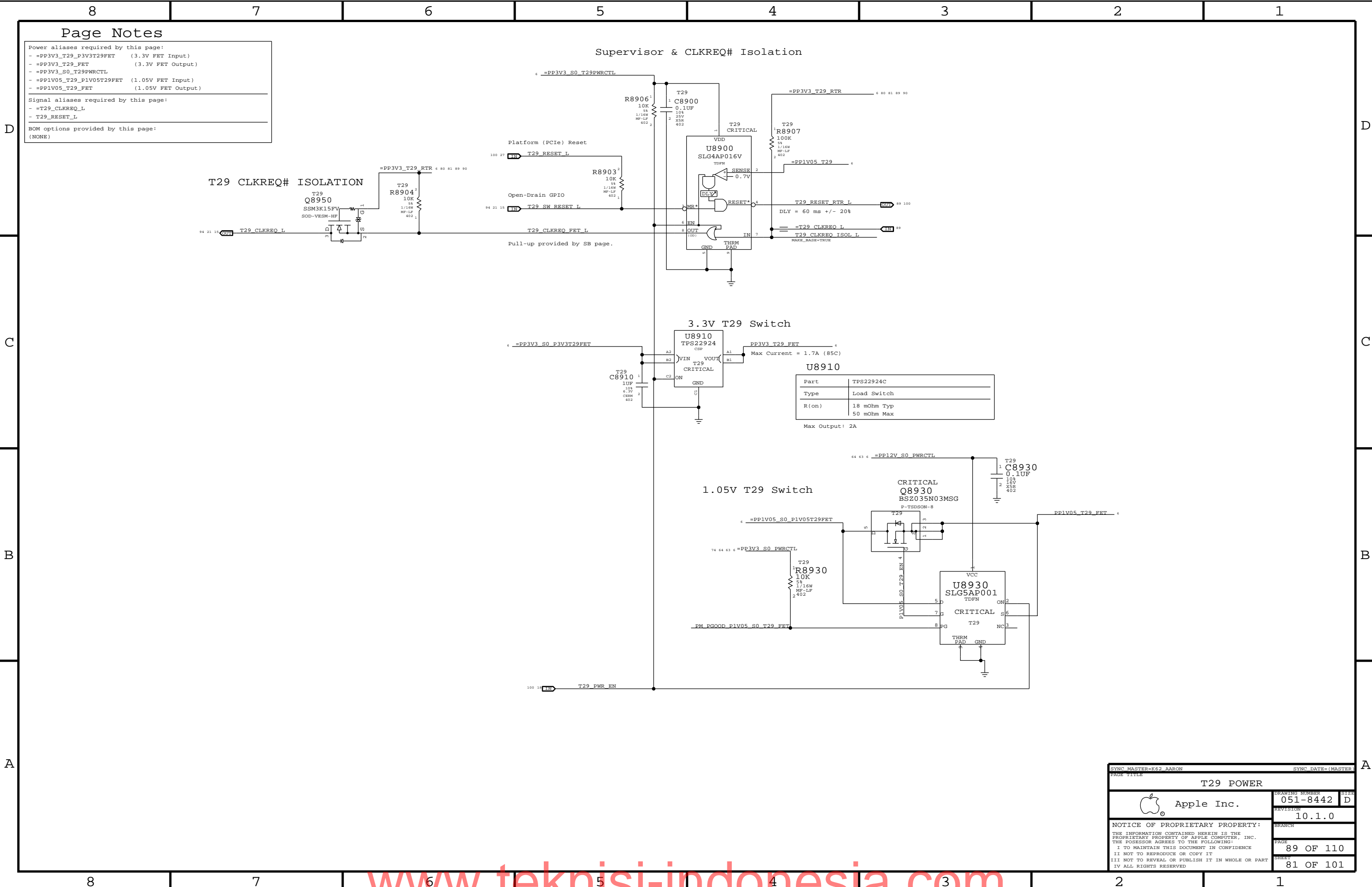
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

System RTC Power Source & 32kHz / 25MHz Clock Generator



| | | | |
|--|----------------|---------------|-------|
| SYNC MASTER=K62 AARON | | SYNC DATE=N/A | |
| PAGE TITLE | | | |
| GREEN CLOCK | | | |
|  Apple Inc. | DRAWING NUMBER | | SHEET |
| | 051-8442 | | D |
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| | | 10.1.0 | |
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| PAGE | | | |
| 88 OF 110 | | | |
| SHEET | | | |
| 80 OF 101 | | | |



Page Notes

Power aliases required by this page:


- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:

- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:

(NONE)

| | | | |
|---|----------------|--------------------|-------|
| SYNC MASTER=K62 AARON | | SYNC DATE=(MASTER) | |
| PAGE TITLE | | | |
| T29 POWER | | | |
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| | | 89 OF 110 | |
| SHEET | | | |
| 81 OF 101 | | | |

Page Notes

Power aliases required by this page:

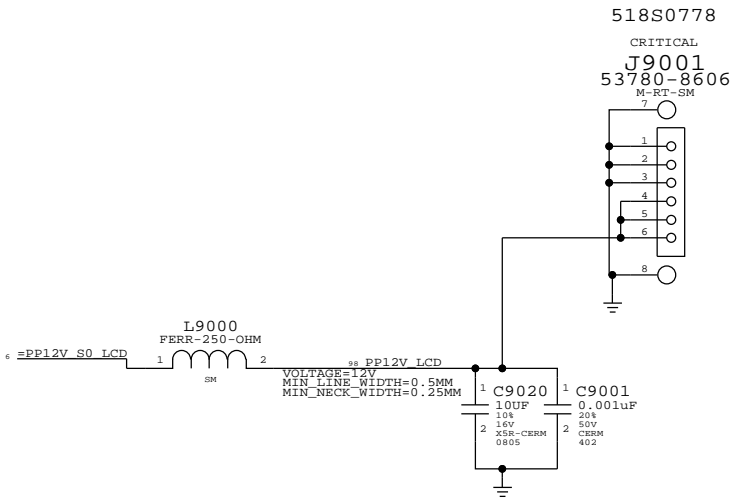
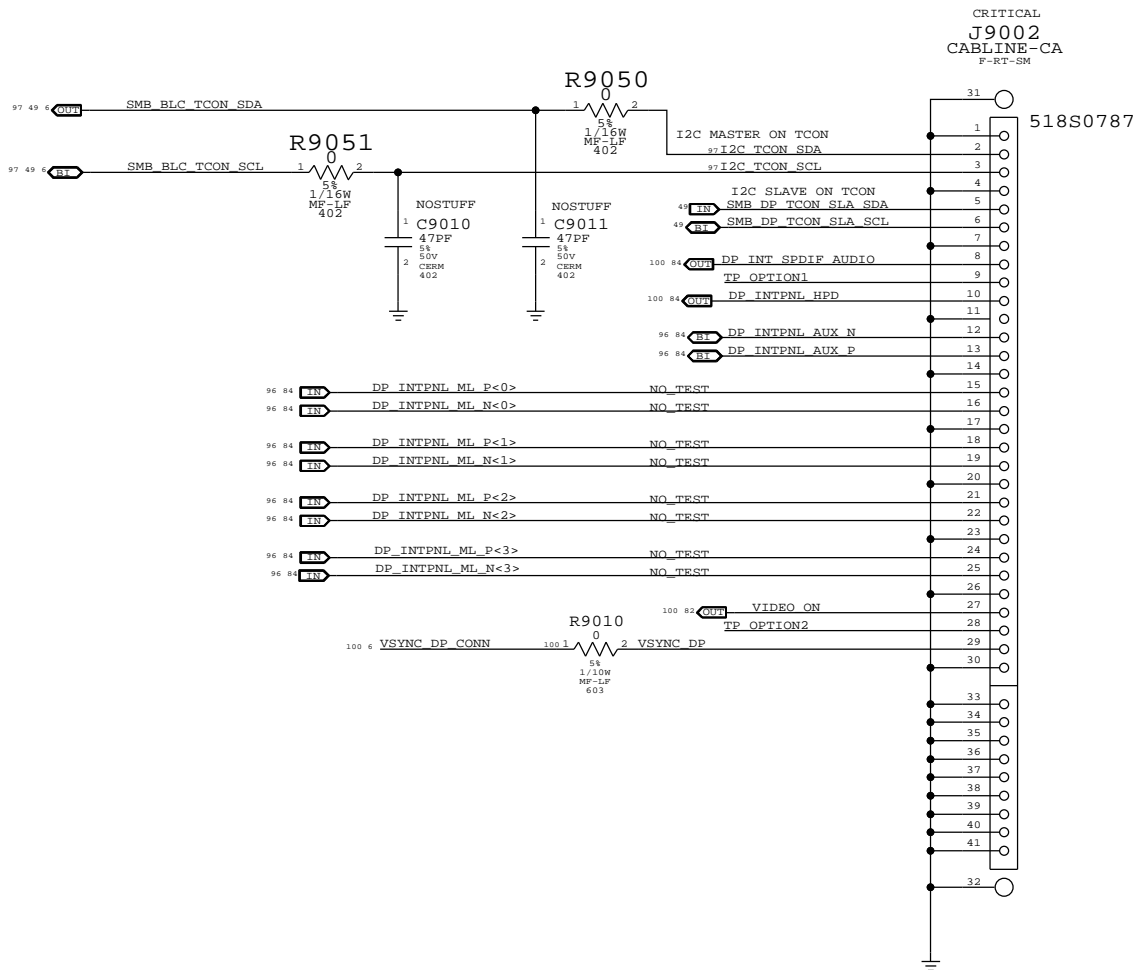
- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

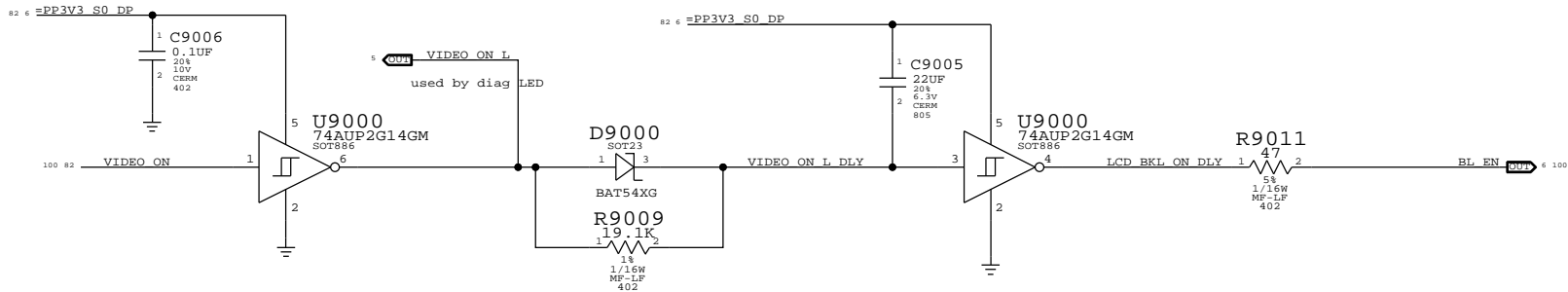
INTERNAL DP INTERFACE


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



| | | | |
|---|--|----------------|-----------|
| SYNC MASTER=K62 AARON | | SYNC DATE=N/A | |
| PAGE TITLE | | | |
| Display: Int DP Connector | | | |
|  Apple Inc. | | DRAWING NUMBER | 051-8442 |
| | | REVISION | 10.1.0 |
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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|



C

B



| | | | |
|---|---|---|---|
| 4 | 3 | 2 | 1 |
|---|---|---|---|



(*) U9410 tolerance unknown ^{T29}_{D910}

C

| | | | |
|-----|--|--|---|
| T29 | | (*) U9410 tolerance unknown T29 D9106 | B |
|-----|--|--|---|

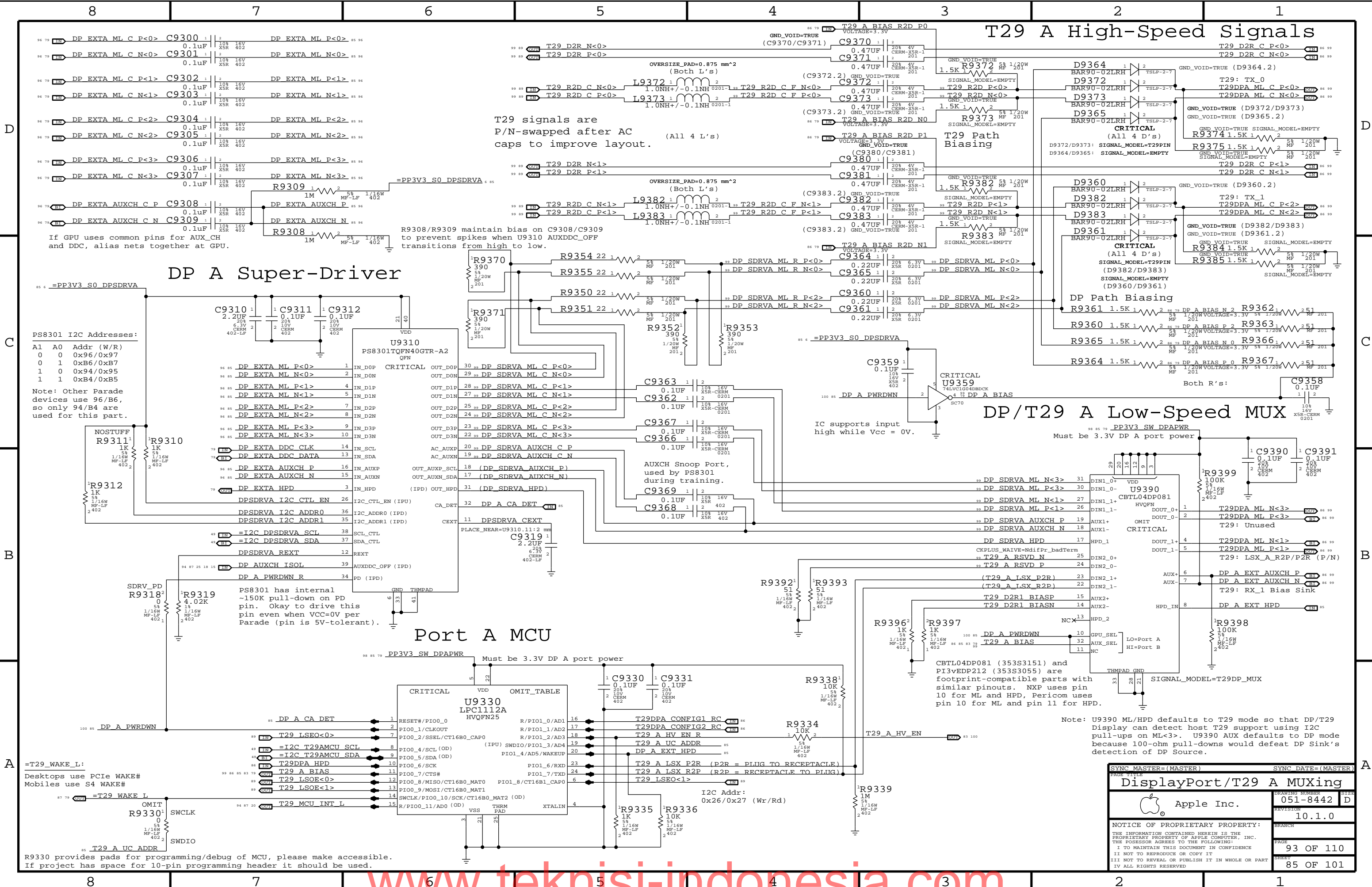


D9106
DCM2

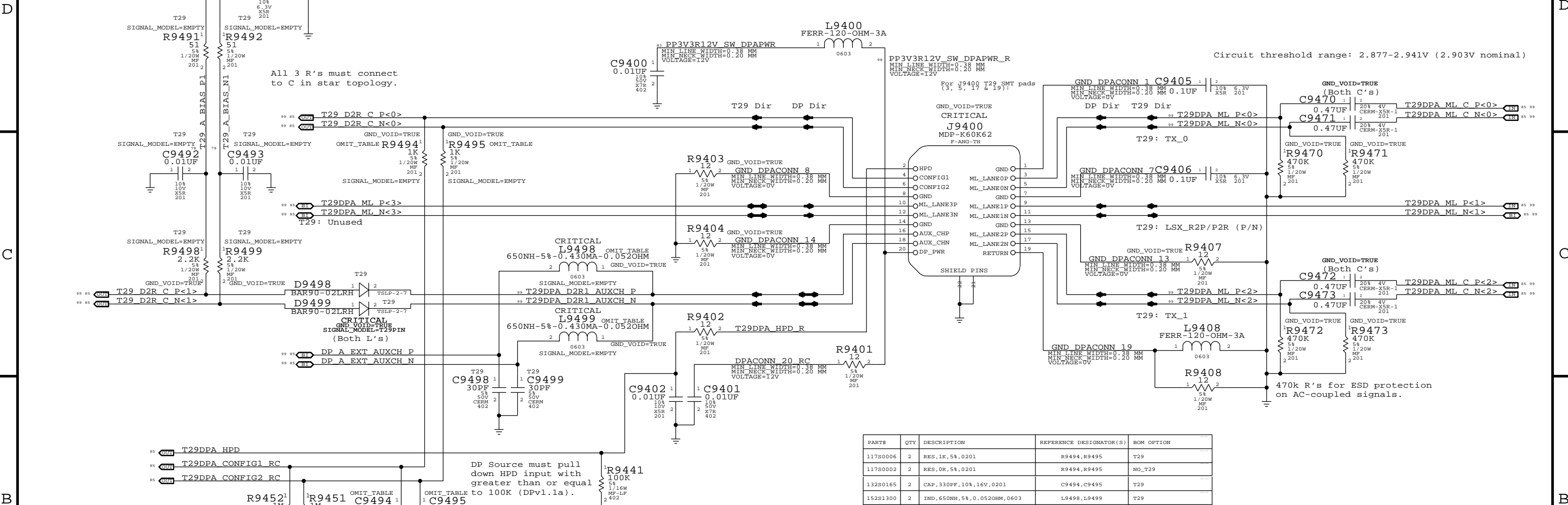
A

www.teknisi-indonesia.com





| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|



The image displays four circuit diagrams for a T29 tube, each showing a different biasing configuration. The diagrams are arranged in a 2x2 grid. Each diagram includes a 51 ohm resistor (R9410, R9412, R9411, R9413) and a 0.01uF capacitor (C9410, C9412, C9411, C9413) connected to the T29 grid. The diagrams are labeled 'T29 A BIAS', 'T29 A BIAS R2D P0', 'T29 A BIAS R2D N0', and 'T29 A BIAS R2D N1'. All diagrams specify 'VOLTAGE=3.3V' and 'SIGNAL_MODEL=EMPTY'.


DP A BIAS P 0
VOLTAGE=3.3V
C9414 0.01uF
10V
XSR 2
SIGNAL_MODEL=EMPTY

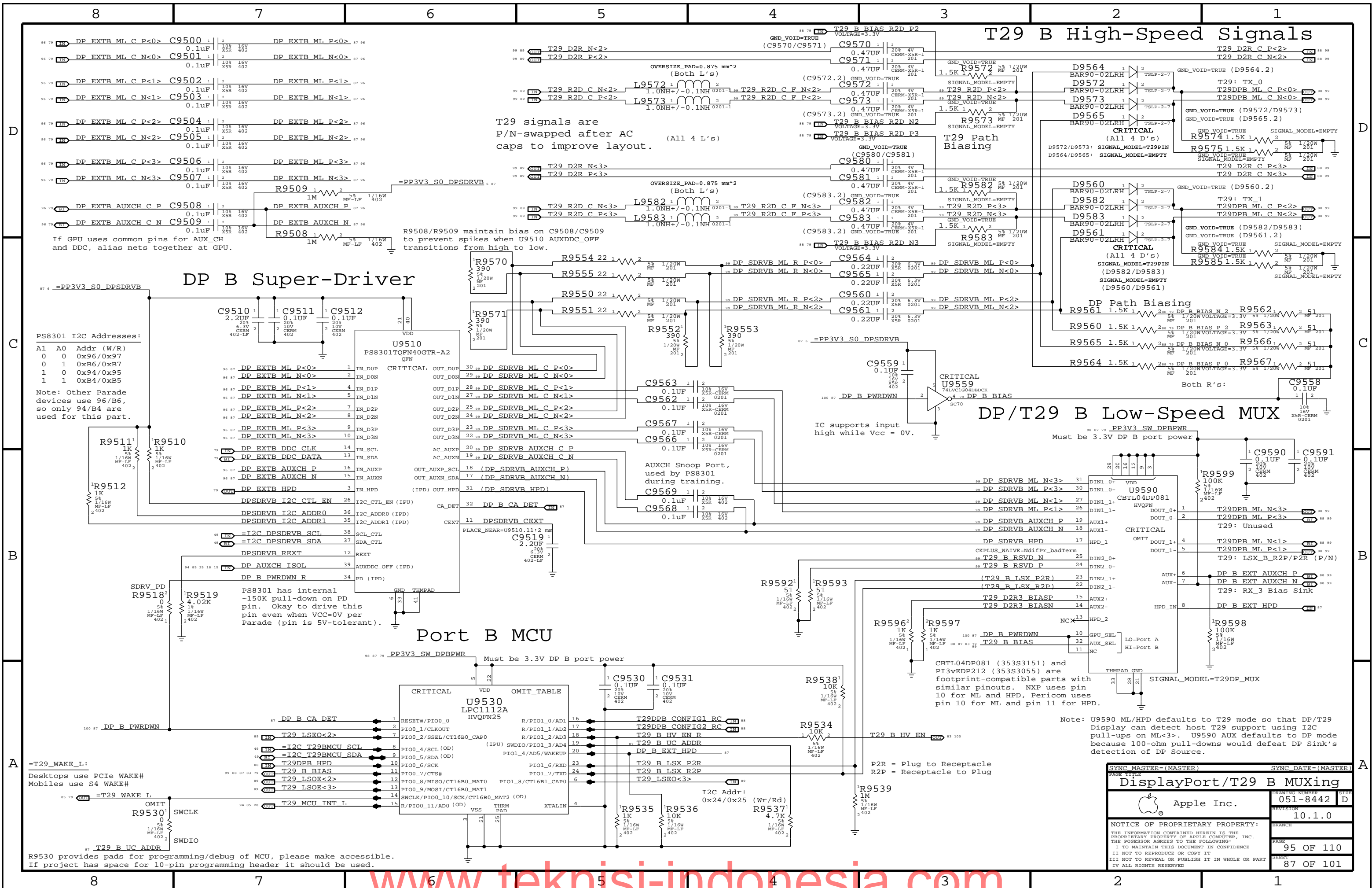
DP A BIAS N 0
VOLTAGE=3.3V
C9415 0.01uF
10V
XSR 2
SIGNAL_MODEL=EMPTY

DP A BIAS P 2
VOLTAGE=3.3V
C9416 0.01uF
10V
XSR 2
SIGNAL_MODEL=EMPTY

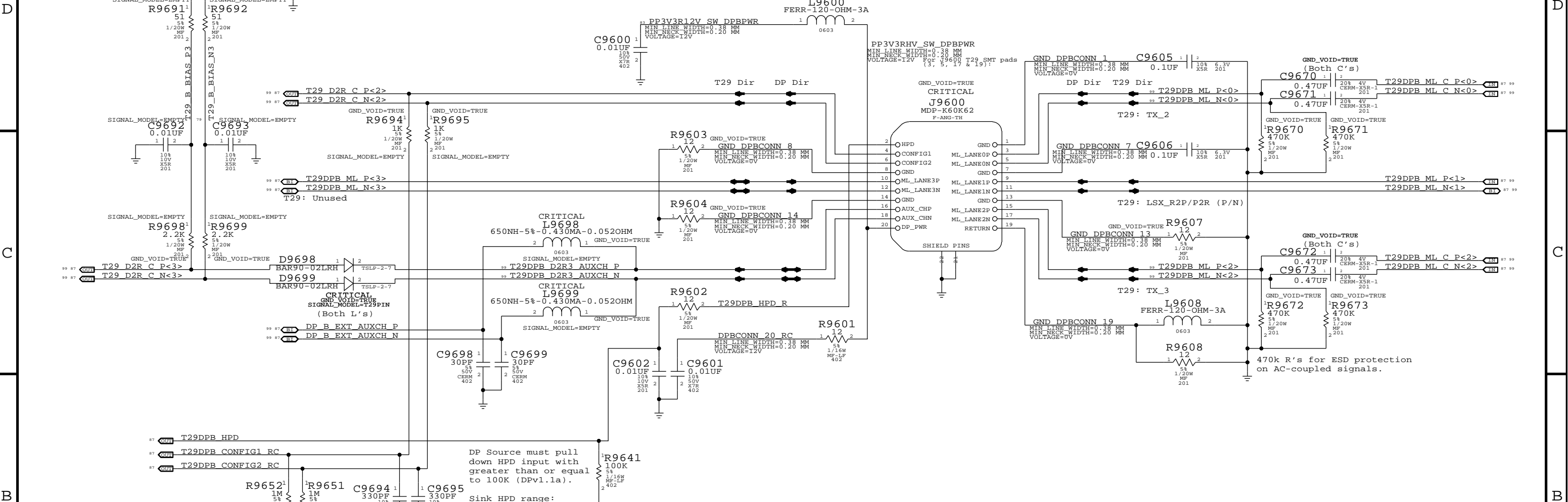
DP A BIAS N 2
VOLTAGE=3.3V
C9417 0.01uF
10V
XSR 2
SIGNAL_MODEL=EMPTY

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|----------------------------|-------------------------|------------|
| 117S0006 | 2 | RES,1K,5%,0201 | R9494,R9495 | T29 |
| 117S0002 | 2 | RES,0R,5%,0201 | R9494,R9495 | NO_T29 |
| 132S0165 | 2 | CAP,330PF,10%,16V,0201 | C9494,C9495 | T29 |
| 152S1300 | 2 | IND,650NH,5%,0.052OHM,0603 | L9498,L9499 | T29 |
| 113S0022 | 2 | RES,0R,5%,0603 | L9498,L9499 | NO_T29 |

| | | | |
|---|--|-----------------------------------|--|
| SYMC MASTER=(MASTER) | | SYMC DATE=(MASTER) | |
| PAGE TITLE | | | |
| DisplayPort/T29 A Connector | | | |
|  Apple Inc. | | DRAWING NUMBER 051-8442 | |
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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|



T29 BIAS RC

The image displays two circuit diagrams for the T29 BIAS RC network. Both diagrams are annotated with 'SIGNAL_MODEL=EMPTY' and 'VOLTAGE=3.3V'.

Left Diagram:

- Top Section:** A network consisting of a 1/20W resistor (R9610) in series with a 0.01uF capacitor (C9610). The resistor is labeled with '1 51 2' and '1/20W MF 201'. The capacitor is labeled with '1 10V 2' and '10V XSR 201'.
- Bottom Section:** A network consisting of a 1/20W resistor (R9611) in series with a 0.01uF capacitor (C9611). The resistor is labeled with '1 51 2' and '1/20W MF 201'. The capacitor is labeled with '1 10V 2' and '10V XSR 201'.
- Connections:** The top section is connected to the bottom section via a 5V source (labeled '5V') and a 1/20W resistor (labeled '1 51 2' and '1/20W MF 201').

Right Diagram:

- Top Section:** A network consisting of a 1/20W resistor (R9612) in series with a 0.01uF capacitor (C9612). The resistor is labeled with '1 51 2' and '1/20W MF 201'. The capacitor is labeled with '1 10V 2' and '10V XSR 201'.
- Bottom Section:** A network consisting of a 1/20W resistor (R9613) in series with a 0.01uF capacitor (C9613). The resistor is labeled with '1 51 2' and '1/20W MF 201'. The capacitor is labeled with '1 10V 2' and '10V XSR 201'.
- Connections:** The top section is connected to the bottom section via a 5V source (labeled '5V') and a 1/20W resistor (labeled '1 51 2' and '1/20W MF 201').

DP BIAS CAPS

87 79 DP_B_BIAS_P_0
VOLTAGE=3.3V

87 79 DP_B_BIAS_N_0
VOLTAGE=3.3V

87 79 DP_B_BIAS_P_2
VOLTAGE=3.3V

87 79 DP_B_BIAS_N_2
VOLTAGE=3.3V

C9614 1
0.01UF
10%
10V
X5R
201
2
SIGNAL_MODEL=EMPTY

C9615 1
0.01UF
10%
10V
X5R
201
2
SIGNAL_MODEL=EMPTY

C9616 1
0.01UF
10%
10V
X5R
201
2
SIGNAL_MODEL=EMPTY

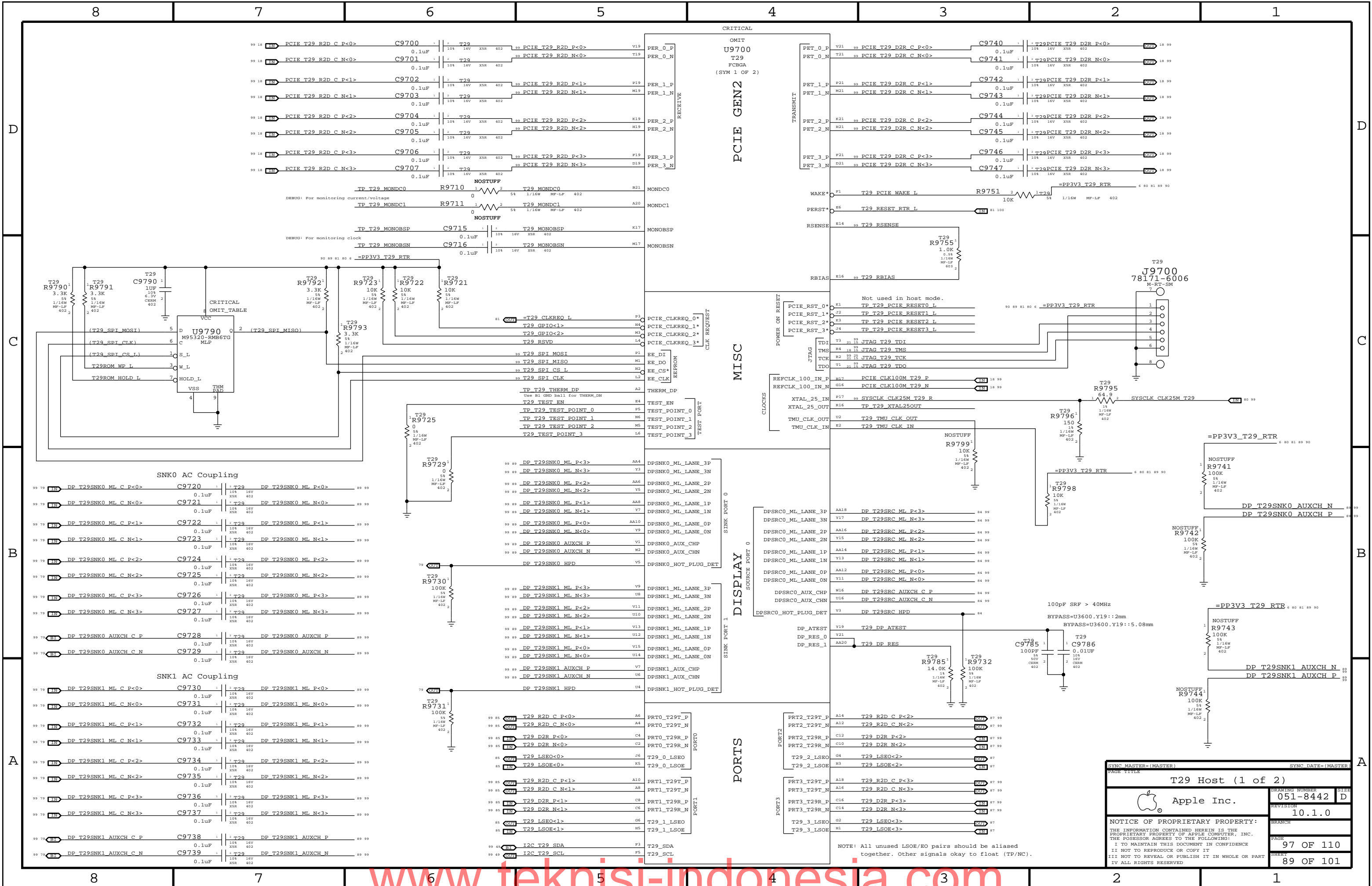
C9617 1
0.01UF
10%
10V
X5R
201
2
SIGNAL_MODEL=EMPTY

Diagram 1 (Left):

- VOLTAGE=3.3V
- 5V
- 1/20W
- 0.01uF
- 10V
- SIGNAL_MODEL=EMPTY

Diagram 2 (Right):

- VOLTAGE=3.3V
- 5V
- 1/20W
- 0.01uF
- 10V
- SIGNAL_MODEL=EMPTY





MEMORY BUS CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| MEM_42S | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =STANDARD | =STANDARD |
| MEM_39S | * | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =STANDARD | =STANDARD |
| MEM_34S | * | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =STANDARD | =STANDARD |
| MEM_68D | * | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF |
| MEM_42S_D | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | 0.1016 MM | 0.1016 MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MEM_CLK2MEM | * | =5:1_SPACING | ? |
| MEM_CTRL2CTRL | * | =2.5:1_SPACING | ? |
| MEM_CTRL2MEM | * | =3.5:1_SPACING | ? |
| MEM_CMD2CMD | * | =2:1_SPACING | ? |
| MEM_CMD2MEM | * | =3.5:1_SPACING | ? |
| MEM_DQ_SAMEBYTE | * | =3:1_SPACING | ? |
| MEM_DQ_DIFFBYTE | * | =5:1_SPACING | ? |
| MEM_DATA2MEM | * | =4:1_SPACING | ? |
| MEM_DQS2MEM | * | =4:1_SPACING | ? |
| MEM_2OTHER | * | =5:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK | MEM_CLK | * | MEM_CLK2MEM |
| MEM_CLK | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CMD | MEM_CTRL | * | MEM_CMD2MEM |
| MEM_CMD | MEM_CMD | * | MEM_CMD2CMD |
| MEM_CMD | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CTRL | MEM_CTRL | * | MEM_CTRL2CTRL |
| MEM_CTRL | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQS | MEM_CTRL | * | MEM_DQS2MEM |
| MEM_DQS | MEM_CMD | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE0 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE1 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE2 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE3 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE4 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE5 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE6 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE7 | * | MEM_DQS2MEM |
| MEM_DQS | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE5 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE5 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE5 | MEM_DQ_BYTE5 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE5 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE5 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE5 | * | * | MEM_ZOTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE6 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE6 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE6 | MEM_DQ_BYTE6 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE6 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE6 | * | * | MEM_ZOTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE7 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE7 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE7 | MEM_DQ_BYTE7 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE7 | * | * | MEM_2OTHER |

Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE0 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE0 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE0 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE1 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE2 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE3 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE1 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE1 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE1 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE2 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE3 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | * | * | MEM_ZOTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE2 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE2 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE2 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE3 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | * | * | MEM_ZOTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE3 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE3 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE3 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | * | * | MEM_ZOTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQ_BYTE4 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE4 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE4 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE4 | * | * | MEM_ZOTHER |

Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | |
|---------------------------|--|-----------|--------------|--------------------------|
| | | PHYSICAL | SPACING | |
| | | MEM_68D | MEM_CLK | MEM A CLK P<3..0> 12 32 |
| | | MEM_68D | MEM_CLK | MEM A CLK N<3..0> 12 32 |
| | | MEM_39S | MEM_CTR1 | MEM A CKR<3..0> 12 30 |
| | | MEM_39S | MEM_CTR1 | MEM A CS L<3..0> 12 30 |
| | | MEM_39S | MEM_CTR1 | MEM A ODT<3..0> 12 30 |
| | | MEM_34S | MEM_CMO | MEM A A<15..0> 12 30 |
| | | MEM_34S | MEM_CMO | MEM A BA<2..0> 12 30 |
| | | MEM_34S | MEM_CMO | MEM A PAS L 12 30 |
| | | MEM_34S | MEM_CMO | MEM A CAS L 12 30 |
| | | MEM_34S | MEM_CMO | MEM A WE L 12 30 |
| | | MEM_42S | MEM_DQ_BVTE0 | MEM A DQ<7..0> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE1 | MEM A DQ<15..8> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE2 | MEM A DQ<23..16> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE3 | MEM A DQ<31..24> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE4 | MEM A DQ<39..32> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE5 | MEM A DQ<47..40> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE6 | MEM A DQ<55..48> 12 32 |
| | | MEM_42S | MEM_DQ_BVTE7 | MEM A DQ<63..56> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<0> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<0> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<1> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<1> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<2> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<2> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<3> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<3> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<4> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<4> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<5> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<5> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<6> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<6> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS P<7> 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM A DQS N<7> 12 32 |
| BMV | | MEM_50R | RM | MEM RESET L 30 31 32 100 |


MEMORY MISC PROPERTIES

| | | NET_TYPE | | |
|--|---------|---------------|-----------|-------------------------|
| | VOLTAGE | PHYSICAL | SPACING | VOLTAGE |
| | | MEM_POWER_PHY | MEM_POWER | CPU_DIMM_VREF_A |
| | | MEM_POWER_PHY | MEM_POWER | CPU_DIMM_VREF_B |
| | | MEM_POWER_PHY | MEM_POWER | CPU_DDR_VREF |
| | | MEM_POWER_PHY | MEM_POWER | VREFMARGIN_DIMMA_DACOUT |
| | | MEM_POWER_PHY | MEM_POWER | VREFMARGIN_DIMMA_OPFB |
| | | MEM_POWER_PHY | MEM_POWER | VREFMARGIN_DIMMA_DO |
| | | MEM_POWER_PHY | MEM_POWER | CPU_DIMM_VREF_A_SW |
| | | MEM_POWER_PHY | MEM_POWER | VREFMARGIN_DIMMB_DACOUT |
| | | MEM_POWER_PHY | MEM_POWER | VREFMARGIN_DIMMB_OPFB |
| | | MEM_POWER_PHY | MEM_POWER | VREFMARGIN_DIMMB_DO |
| | | MEM_POWER_PHY | MEM_POWER | CPU_DIMM_VREF_B_SW |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_POWER_WIDTH | * | Y | 0.500 MM | 0.250 MM | =STANDARD | =STANDARD | =STANDARD |

| | | | | | | |
|-------------------|-----------|-------------------|------------------|-------|----------------------|--------|
| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
| MEM_POWER_PHY | * | MEM_POWER_WIDTH | MEM_POWER | * | =3:1_SPACING | ? |

| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | | |
|---------------------------|-----------|-----------|----------------|-------------------|-------|
| | | PHYSICAL | SPACING | | |
| □□ | | MEM_68D | MEM_CLK | MEM B CLK P<3..0> | 12 32 |
| | | MEM_68D | MEM_CLK | MEM B CLK N<3..0> | 12 32 |
| □□□ | | MEM_39S | MEM_CTL1 | MEM B CKR<3..0> | 12 31 |
| | | MEM_39S | MEM_CTL1 | MEM B CS L<3..0> | 12 31 |
| | | MEM_39S | MEM_CTL1 | MEM B ODT<3..0> | 12 |
| □□□□ | | MEM_34S | MEM_CMD | MEM B A<15..0> | 12 31 |
| | | MEM_34S | MEM_CMD | MEM B BA<2..0> | 12 31 |
| | | MEM_34S | MEM_CMD | MEM B RAS L | 12 31 |
| | | MEM_34S | MEM_CMD | MEM B CAS L | 12 31 |
| | | MEM_34S | MEM_CMD | MEM B WE L | 12 31 |
| □□□□□ | | MEM_42S | MEM_DQ_BVTF0 | MEM B DQ<7..0> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF1 | MEM B DQ<15..8> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF2 | MEM B DQ<23..16> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF3 | MEM B DQ<31..24> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF4 | MEM B DQ<39..32> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF5 | MEM B DQ<47..40> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF6 | MEM B DQ<55..48> | 12 32 |
| | | MEM_42S | MEM_DQ_BVTF7 | MEM B DQ<63..56> | 12 32 |
| □□□□□□ | | MEM_42S_D | MEM_DQS | MEM B DQS P<0> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<0> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<1> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<1> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<2> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<2> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<3> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<3> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<4> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<4> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<5> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<5> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<6> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS N<6> | 12 32 |
| | | MEM_42S_D | MEM_DQS | MEM B DQS P<7> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM B DQS N<7> | 12 32 | |

| | | | |
|---|----------------|-----------------------|------|
| SYNCH MASTER=K62 ROSITA | | SYNCH DATE=01/09/2011 | |
| PAGE TITLE | | | |
| Memory Constraints | | | |
|  Apple Inc. | DRAWING NUMBER | | SIZE |
| | 051-8442 | | D |
| REVISION | | 10.1.0 | |
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PCI-Express

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| CLK_PCIE_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| PCIE | * | =4X_DIELECTRIC | ? | PCIE | TOP,BOTTOM | =4:1_SPACING | ? |
| CLK_PCIE | * | 0.5 MM | ? | | | | |

CPU

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CPU_RCOMP_PHY | * | Y | 0.254 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|-------|----------------------|--------|
| CPU_ITP | * | 0.2 MM | ? | | | | |
| CPU_RCOMP | * | 0.2 MM | ? | | | | |

SATA Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SATA_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| SATA | * | =6:1_SPACING | ? | SATA | TOP,BOTTOM | =6:1_SPACING | ? |

| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | | |
|---------------------------|--|---------------|-----------|---------------------|----------|
| SATA | | PHYSICAL | SPACING | | |
| H300 | | SATA_90D | SATA | SATA SSD R2D C P | 18 42 |
| H300 | | SATA_90D | SATA | SATA SSD R2D C N | 18 42 |
| H300 | | SATA_90D | SATA | SATA SSD R2D P | 42 |
| H300 | | SATA_90D | SATA | SATA SSD R2D N | 42 |
| H300 | | SATA_90D | SATA | SATA SSD D2R P | 18 42 |
| H300 | | SATA_90D | SATA | SATA SSD D2R N | 18 42 |
| H300 | | SATA_90D | SATA | SATA SSD D2R C P | 42 |
| H300 | | SATA_90D | SATA | SATA SSD D2R C N | 42 |
| PCIE | | | | | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 R2D P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 R2D N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 R2D C P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 R2D C N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 D2R P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 D2R N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 D2R C P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 1 D2R C N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 R2D P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 R2D N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 R2D C P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 R2D C N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 D2R P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 D2R N | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 D2R C P | |
| H300 | | PCIE_85D | PCIE | PCIE USB3 2 D2R C N | |
| CPU ITP | | | | | |
| H300 | | CPU_50S | CPU_ITP | XDP BPM L<7..0> | 11 25 |
| H300 | | CPU_50S | CPU_ITP | CPU CFG<17..0> | 10 15 25 |
| H300 | | CPU_50S | CPU_ITP | XDP OBSDATA B<3..0> | 25 |
| H300 | | CPU_50S | CPU_ITP | XDP CPU CFG<0> | 25 |
| H300 | | CPU_50S | CPU_ITP | XDP CPU TDO | 11 25 |
| H300 | | CPU_50S | CPU_ITP | XDP CPU TDI | 11 25 |
| H300 | | CPU_50S | CPU_ITP | XDP CPU TMS | 11 25 |
| H300 | | CPU_50S | CPU_ITP | XDP CPU TCK | 11 25 |
| H300 | | CPU_50S | CPU_ITP | XDP CPU TRST L | 11 25 |
| CPU_MISC | | | | | |
| H300 | | CPU_RCOMP_PHY | CPU_RCOMP | CPU PEG COMP | 10 |

| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | | |
|---------------------------|--|--------------|----------|-----------------------|-------|
| PCIE GRAPHICS | | PHYSICAL | SPACING | | |
| H300 | | PCIE_85D | PCIE | PEG R2D C P<15..0> | 9 78 |
| H300 | | PCIE_85D | PCIE | PEG R2D C N<15..0> | 9 78 |
| H300 | | PCIE_85D | PCIE | PEG D2R P<15..0> | 9 78 |
| H300 | | PCIE_85D | PCIE | PEG D2R N<15..0> | 9 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE R2D P<7..0> | 76 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE R2D N<7..0> | 76 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE D2R P<7..0> | 76 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE D2R N<7..0> | 76 78 |
| PCIE I/O | | | | | |
| H300 | | PCIE_85D | PCIE | PCIE MINI R2D P | 33 |
| H300 | | PCIE_85D | PCIE | PCIE MINI R2D N | 33 |
| H300 | | PCIE_85D | PCIE | PCIE MINI R2D C P | 18 33 |
| H300 | | PCIE_85D | PCIE | PCIE MINI R2D C N | 18 33 |
| H300 | | PCIE_85D | PCIE | PCIE MINI D2R P | 18 33 |
| H300 | | PCIE_85D | PCIE | PCIE MINI D2R N | 18 33 |
| DMI | | | | | |
| H300 | | CLK_PCIE_90D | CLK_PCIE | DMI MIDBUS CLK100M N | |
| H300 | | CLK_PCIE_90D | CLK_PCIE | DMI MIDBUS CLK100M P | |
| H300 | | CLK_PCIE_90D | CLK_PCIE | DMI CLK100M CPU N | 11 18 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | DMI CLK100M CPU P | 11 18 |
| H300 | | PCIE_85D | PCIE | DMI S2N P<3..0> | 10 19 |
| H300 | | PCIE_85D | PCIE | DMI S2N N<3..0> | 10 19 |
| H300 | | PCIE_85D | PCIE | DMI N2S P<3..0> | 10 19 |
| H300 | | PCIE_85D | PCIE | DMI N2S N<3..0> | 10 19 |
| PCIE REF CLOCKS | | | | | |
| H300 | | CLK_PCIE_90D | CLK_PCIE | GPU CLK100M PCIE P | 9 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | GPU CLK100M PCIE N | 9 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCIE CLK100M MINI P | 18 33 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCIE CLK100M MINI N | 18 33 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCIE CLK100M FW P | 18 39 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCIE CLK100M FW N | 18 39 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCIE CLK100M ENET P | 18 39 |
| H300 | | ENET_100D | ENET_MII | PCIE CLK100M ENET P | 18 37 |
| H300 | | ENET_100D | ENET_MII | PCIE CLK100M ENET N | 18 37 |
| SATA | | | | | |
| H300 | | SATA_90D | SATA | SATA HDD R2D C P | 18 42 |
| H300 | | SATA_90D | SATA | SATA HDD R2D C N | 18 42 |
| H300 | | SATA_90D | SATA | SATA HDD R2D P | 42 |
| H300 | | SATA_90D | SATA | SATA HDD R2D N | 42 |
| H300 | | SATA_90D | SATA | SATA HDD D2R P | 18 42 |
| H300 | | SATA_90D | SATA | SATA HDD D2R N | 18 42 |
| H300 | | SATA_90D | SATA | SATA HDD D2R C P | 42 |
| H300 | | SATA_90D | SATA | SATA HDD D2R C N | 42 |
| H300 | | SATA_90D | SATA | SATA ODD R2D C P | 18 42 |
| H300 | | SATA_90D | SATA | SATA ODD R2D C N | 18 42 |
| H300 | | SATA_90D | SATA | SATA ODD R2D P | 42 |
| H300 | | SATA_90D | SATA | SATA ODD R2D N | 42 |
| H300 | | SATA_90D | SATA | SATA ODD D2R P | 18 42 |
| H300 | | SATA_90D | SATA | SATA ODD D2R N | 18 42 |
| H300 | | SATA_90D | SATA | SATA ODD D2R C P | 42 |
| H300 | | SATA_90D | SATA | SATA ODD D2R C N | 42 |
| CLOCKS | | | | | |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCH CLK100M DMI P | 18 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCH CLK100M DMI N | 18 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCH CLK96M DOT P | 18 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCH CLK96M DOT N | 18 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCH CLK100M SATA P | 18 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | PCH CLK100M SATA N | 18 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | ITPXD P CLK100M N | 18 25 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | ITPXD P CLK100M P | 18 25 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | ITPCPU CLK100M N | 11 18 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | ITPCPU CLK100M P | 11 18 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | XDP CPU CLK100M P | 25 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | XDP CPU CLK100M N | 25 |
| UNUSED CLOCKS | | | | | |
| H300 | | CLK_PCIE_90D | CLK_PCIE | TP CLK133M PCH N | 26 |
| H300 | | CLK_PCIE_90D | CLK_PCIE | TP CLK133M PCH P | 26 |
| UNUSED PCIE | | | | | |
| H300 | | PCIE_85D | PCIE | MXM PCIE R2D P<8..15> | 76 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE R2D N<8..15> | 76 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE D2R P<8..15> | 76 78 |
| H300 | | PCIE_85D | PCIE | MXM PCIE D2R N<8..15> | 76 78 |

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

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SYNC DATE=01/09/2011

PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCH_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCH_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_PCH | * | =4:1_SPACING | ? |
| COMP_PCH | * | 0.2 MM | ? |
| ITP_PCH | * | 0.2 MM | ? |

PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCI | * | =STANDARD | ? |
| CLK_PCI | * | 0.2 MM | ? |

LPC Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| LPC | * | 0.15 MM | ? |
| CLK_LPC | * | 0.2 MM | ? |

SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB | * | =2x_DIELECTRIC | ? |

HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| HDA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| HDA | * | =2x_DIELECTRIC | ? |

SPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SPI | * | 0.2 MM | ? |

XTAL Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_XTAL | * | -100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |


| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| XTAL | * | =4X_DIELECTRIC | ? |

| PHYSICAL | | NET_TYPE | SPACING | |
|----------|----|---------------------|---------|-------------|
| SW0 | PM | T29 CLKREQ L | 16 | 21 81 |
| SW1 | PM | FW MINI_CLKREQ L | 16 | 16 |
| SW2 | PM | BLC GPIO | 4 | 18 21 |
| SW3 | PM | T29_SW RESET L | 16 | 21 91 |
| SW4 | PM | ENET CLKREQ L | 16 | 18 36 |
| SW5 | PM | DP GPU T29 SEL | 16 | 41 84 |
| SW6 | PM | T29 MCU INT L | 20 | 85 87 |
| SW7 | PM | T29_DP PORTA PWR_EN | 20 | 25 83 100 |
| SW8 | PM | T29_DP PORTB PWR_EN | 20 | 25 83 |
| SW9 | PM | DP AUXCH ISOL | 16 | 18 25 85 87 |
| SW10 | PM | PLT_RST BUF L | | 27 |
| SW11 | PM | XDPCPU_PLTRST L | | 26 27 |
| SW12 | PM | PCH PGW CLKREQ L | | 21 |
| SW13 | PM | ENET_SW RESET L | 16 | 21 36 |
| SW14 | PM | CPU_SKT0CC | | 63 |
| SW15 | PM | PM_EN_USB_PWR | | 43 63 |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|-------------|---------|----------------------|----------|
| | PHYSICAL | SPACING | | |
| | PCI_558 | PCI | PCI REQ0 L | 20 |
| | PCI_558 | PCI | PCI REQ1 L | 20 |
| | PCI_558 | PCI | PCI REQ2 L | 20 |
| | CLK_PCI_558 | CLK_PCI | PCH CLK33M PCIOUT | 20 27 |
| | CLK_PCI_558 | CLK_PCI | PCH CLK33M PCIIIN | 18 27 |
| | LPC_558 | LPC | LPC AD<3..0> | 18 46 48 |
| | LPC_558 | LPC | LPC FRAME L | 18 46 48 |
| | CLK_LPC_558 | CLK_LPC | LPC CLK33M SMC R | 20 27 |
| | CLK_LPC_558 | CLK_LPC | LPC CLK33M SMC | 27 46 |
| | CLK_LPC_558 | CLK_LPC | LPC CLK33M LPCPLUS | 27 48 |
| | CLK_LPC_558 | PM | PM CLK32K SUSCLK R | 9 19 100 |
| | CLK_LPC_558 | PM | PM CLK32K SUSCLK | 9 46 100 |
| | CLK_LPC_558 | CLK_LPC | LPC CLK33M LPCPLUS R | 20 27 |
| | LPC_558 | LPC | LPC R AD<3..0> | 18 |
| | LPC_558 | LPC | LPC FRAME R L | 18 |
| | SPI_558 | SPI | SPI CLK 1 R | 18 |
| | SPI_558 | SPI | SPI MOSI 1 R | 18 |
| | CLK_XTAL | XTAL | USB HUB2 XTAL1 | 35 |
| | CLK_XTAL | XTAL | USB HUB2 XTAL2 | 35 |
| | CLK_XTAL | XTAL | PCH CLK32K RTCX1 R | 27 |
| | CLK_XTAL | XTAL | PCH CLK32K RTCX2 R | 27 |
| | CLK_XTAL | XTAL | PCH CLK32K RTCX1 | 18 27 94 |
| | CLK_XTAL | XTAL | PCH CLK32K RTCX2 | 18 27 94 |
| | CLK_XTAL | XTAL | PCH CLK32K RTCX1 | 18 27 94 |
| | CLK_XTAL | XTAL | PCH CLK32K RTCX2 | 18 27 94 |
| | CLK_XTAL | XTAL | CK505 XTAL IN | 26 |
| | CLK_XTAL | XTAL | CK505 XTAL OUT | 26 |
| | CLK_XTAL | XTAL | CK505 XTAL OUT R | 26 |
| | CLK_PCH_558 | CLK_PCH | PCH CLK14P3M REFCLK | 18 26 |

| | | NET_TYPE | |
|----------|----|------------------------|--------|
| PHYSICAL | | SPACING | |
| RES0 | PM | ENET RESET LOGIC L | 36 |
| RES0 | PM | ENET RESET FET L | |
| RES0 | PM | ENET CLKREQ FET L | 36 37 |
| RES0 | PM | PGOOD 5V 1V05 3V3 | 64 100 |
| RES0 | PM | PGOOD CPU UNCORE | 64 100 |
| RES0 | PM | ALL SYS PWRGD | 64 100 |
| RES0 | PM | PGOOD 3V3 1V05 | 64 100 |
| RES0 | PM | PGOOD PCH S0 R | 64 100 |
| RES0 | PM | AUD IPHS SWITCH EN PCH | 21 25 |

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | NET_TYPE | SPACING | |
|---------------------------|----------|----------|---------|----------------------------|
| | SPI_55S | SPI | | SPI CLK R 18 48 55 |
| | SPI_55S | SPI | | SPI CLK 55 |
| | SPI_55S | SPI | | SPI MOSI R 18 48 55 |
| | SPI_55S | SPI | | SPI MOSI 55 |
| | SPI_55S | SPI | | SPI MISO 18 48 55 |
| | SPI_55S | SPI | | SPI MISO R 55 |
| | SPI_55S | SPI | | SPI CS0 R L 18 48 |
| | SPI_55S | SPI | | SPI CS0 L 48 |
| | SPI_55S | SPI | | SPI MLB CS L 48 55 |
| | SPI_55S | SPI | | SPI ALT CS L 48 |
| | SPI_55S | SPI | | SPIROM USE MLB 21 48 |
| | SPI_55S | SPI | | SPI ALT MOSI 48 |
| | SPI_55S | SPI | | SPI ALT MISO 48 |
| | SPI_55S | SPI | | SPI ALT CLK 48 |
| | HDA_55S | HDA | | HDA BIT CLK 18 56 |
| | HDA_55S | HDA | | HDA BIT CLK R 18 |
| | HDA_55S | HDA | | HDA RST L 18 56 |
| | HDA_55S | HDA | | HDA RST R L 18 |
| | HDA_55S | HDA | | HDA SDOUT 15 18 56 |
| | HDA_55S | HDA | | HDA SDOUT R 18 |
| | HDA_55S | HDA | | HDA SYNC 18 56 |
| | HDA_55S | HDA | | HDA SYNC R 18 |
| | HDA_55S | HDA | | HDA SDINO 18 56 |
| | HDA_55S | HDA | | AUD SDI R 56 |
| | | FW | | AUD SPDIF IN 60 84 100 |
| | | HDA | | AUD SPDIF OUT 56 60 |
| | | HDA | | AUD SPDIF CHIP 56 |
| | HDA_55S | HDA | | AUD SPKR OUTLO1L NOUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO1L POUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO1R NOUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO1R POUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO2L NOUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO2L POUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO2R NOUT 101 |
| | HDA_55S | HDA | | AUD SPKR OUTLO2R POUT 101 |
| RED | CLK_XTAL | XTAL | | PCH CLK25M XTALOUT R 27 |
| RED | CLK_XTAL | XTAL | | PCH CLK25M XTALIN R 27 |
| | CLK_XTAL | XTAL | | PCH CLK25M XTALOUT 18 27 |
| | CLK_XTAL | XTAL | | PCH CLK25M XTALIN 18 27 80 |
| | PCH_55S | COMP_PCH | | PCH USB RBIAS 20 |
| | PCH_55S | COMP_PCH | | PCH SATA3COMP 18 |
| | PCH_55S | COMP_PCH | | PCH SATA3COMP 18 |
| | PCH_55S | COMP_PCH | | PCH XCLK RCOMP 18 |
| | PCH_55S | COMP_PCH | | PCH DMI COMP 19 |
| | PCH_55S | COMP_PCH | | PCH SATA3COMP 18 |
| | CLK_XTAL | XTAL | | USB HUB1 XTAL1 34 |
| | CLK_XTAL | XTAL | | USB HUB1 XTAL2 34 |
| | PCH_55S | COMP_PCH | | USB HUB1 RBIAS 34 |
| | PCH_55S | ITP_PCH | | XDP PCH TCK 18 25 |
| | PCH_55S | ITP_PCH | | XDP PCH TMS 18 25 |
| | PCH_55S | ITP_PCH | | XDP PCH TDI 18 25 |
| | PCH_55S | ITP_PCH | | XDP PCH TDO 18 25 |
| RED | PCH_55S | COMP_PCH | | PCH DMI2RBIA 19 |
| RED | PCH_55S | COMP_PCH | | PCH SATA3RBIA 18 |
| RED | PCH_55S | COMP_PCH | | USB HUB2 RBIA 35 |

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D

C

B

A

SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFFAIR PRIMARY GAP | DIFFFAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB | * | =2x_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| THERMAL | * | * | 4:1_SPACING |
| THERMAL | POWER | * | PWR_P2MM |
| THERMAL | GND | * | GND_P2MM |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| THERM_DIFF | * | 1:1_DIFFPAIR |
| SNS_DIFF | * | 1:1_DIFFPAIR |

SMC SMBus Net Properties


| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | |
|---------------------------|----------|----------|-------------------------|---------|
| | PHYSICAL | SPACING | | |
| | SMB_55R | SMB | SMBUS SMC A S3 SCL | 49 |
| | SMB_55R | SMB | SMBUS SMC A S3 SDA | 49 |
| | SMB_55R | SMB | SMBUS SMC B S0 SCL | 49 |
| | SMB_55R | SMB | SMBUS SMC B S0 SDA | 49 |
| | SMB_55R | SMB | SMBUS SMC 0 S0 SCL | 49 |
| | SMB_55R | SMB | SMBUS SMC 0 S0 SDA | 49 |
| | SMB_55R | SMB | SMBUS SMC BSA SCL | 49 |
| | SMB_55R | SMB | SMBUS SMC BSA SDA | 49 |
| | SMB_55R | SMB | SMBUS SMC MGMT SCL | 49 97 |
| | SMB_55R | SMB | SMBUS SMC MGMT SDA | 49 97 |
| | SMB_55R | SMB | SMBUS SMC MGMT SCL | 49 97 |
| | SMB_55R | SMB | SMBUS SMC MGMT SDA | 49 97 |
| | SMB_55R | SMB | SMBUS PCH CLK | 18 49 |
| | SMB_55R | SMB | SMBUS PCH DATA | 18 49 |
| | SMB_55R | SMB | SML PCH 0 CLK | 18 49 |
| | SMB_55R | SMB | SML PCH 0 DATA | 18 49 |
| | SMB_55R | SMB | SML PCH 1 CLK | 18 49 |
| | SMB_55R | SMB | SML PCH 1 DATA | 18 49 |
| | CLK_XTAL | XTAL | SMC XTAL | 46 47 |
| | CLK_XTAL | XTAL | SMC_XTAL | 46 47 |
| ES04 | SMB_55R | SMB | I2C VREFPFRGN DIMMA SCL | 28 |
| ES05 | SMB_55R | SMB | I2C VREFPFRGN DIMMA SDA | 28 |
| ES06 | SMB_55R | SMB | I2C VREFPFRGN DIMMB SCL | 28 |
| ES07 | SMB_55R | SMB | I2C VREFPFRGN DIMMB SDA | 28 |
| ES08 | SMB_55R | SMB | SMB BLC TCON SCL | 6 49 82 |
| ES09 | SMB_55R | SMB | SMB BLC TCON SDA | 6 49 82 |
| ES10 | SMB_55R | SMB | I2C TCON SCL | 82 |
| ES11 | SMB_55R | SMB | I2C TCON SDA | 82 |
| ES12 | SMB_55R | SMB | SMB BLC PCH SCL R | 6 |
| ES13 | SMB_55R | SMB | SMB BLC PCH SDA R | 6 |

SMC THERMAL NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|------------|---------|-------------------|-----------|
| | PHYSICAL | SPACING | | |
| | THERM_DIEF | THERMAL | SNS_T1_1_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_1_N | 52 |
| | THERM_DIEF | THERMAL | SNS_T2_DP2 | 52 |
| | THERM_DIEF | THERMAL | SNS_T2_DN2 | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_2_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_2_N | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_3_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_3_N | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_4_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_4_N | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_5_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_5_N | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_6_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_6_N | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_7_P | 52 |
| | THERM_DIEF | THERMAL | SNS_T1_7_N | 52 |
| | | | | |
| | THERM_DIEF | THERMAL | SNS_CPU_THERMD_P | 10 52 |
| | THERM_DIEF | THERMAL | SNS_CPU_THERMD_N | 10 52 |
| | THERM_DIEF | THERMAL | SNS_LCD_H_P | 52 |
| | THERM_DIEF | THERMAL | SNS_LCD_H_N | 52 |
| | THERM_DIEF | THERMAL | SNS_ODD_P | 52 101 |
| | THERM_DIEF | THERMAL | SNS_ODD_N | 52 101 |
| | THERM_DIEF | THERMAL | SNS_CPU_H_P | 52 |
| | THERM_DIEF | THERMAL | SNS_CPU_H_N | 52 |
| | THERM_DIEF | THERMAL | SNS_SKIN_RIGHT_P | 52 101 |
| | THERM_DIEF | THERMAL | SNS_SKIN_RIGHT_N | 52 101 |
| | THERM_DIEF | THERMAL | SNS_SKIN_LEFT_P | 44 52 101 |
| | THERM_DIEF | THERMAL | SNS_SKIN_LEFT_N | 44 52 101 |
| | | | | |
| | THERM_DIEF | THERMAL | SNS_AMB_P | 52 101 |
| | THERM_DIEF | THERMAL | SNS_AMB_N | 52 101 |
| | THERM_DIEF | THERMAL | SNS_MXM_P | 52 |
| | THERM_DIEF | THERMAL | SNS_MXM_N | 52 |
| | | | | |
| | | THERMAL | HDD_OOB_TEMP_FILT | 42 51 101 |
| | | THERMAL | HDD_OOB_TEMP_FB | 42 |
| | | THERMAL | HDD_OOB_TEMP_R | 51 |
| | | THERMAL | SMC_HDD_OOB_TEMP | 46 51 |

SMC VOLTAGE/CURRENT NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|------------|---------|----------------------|-------------|
| | PHYSICAL | SPACING | | |
| | THERM_DIFF | THERMAL | SNS I MMX P | 50 |
| | THERM_DIFF | THERMAL | SNS I MMX N | 50 |
| | THERM_DIFF | THERMAL | SNS DIMM 1V5 P | 50 |
| | THERM_DIFF | THERMAL | SNS DIMM 1V5 N | 50 |
| | SNS_DIFF | THERMAL | VR ISNS VCORE P | 50 98 |
| | SNS_DIFF | THERMAL | VR ISNS VCORE N | 50 98 |
| | SNS_DIFF | THERMAL | VR ISNS VAXG P | 50 98 |
| | SNS_DIFF | THERMAL | VR ISNS VAXG N | 50 98 |
| | SNS_DIFF | THERMAL | VR ISNS 1V05 P | 98 |
| | SNS_DIFF | THERMAL | VR ISNS 1V05 N | 98 |
| | THERM_DIFF | THERMAL | SNS CPU 1V5 P | 50 |
| | THERM_DIFF | THERMAL | SNS CPU 1V5 N | 50 |
| | THERM_DIFF | THERMAL | SNS VCCSA P | 50 |
| | THERM_DIFF | THERMAL | SNS VCCSA N | 50 |
| | | | | |
| | THERM_DIFF | THERMAL | SNS 1V05 PCH P | 50 |
| | THERM_DIFF | THERMAL | SNS 1V05 PCH N | 50 |
| | | | | |
| | | THERMAL | GND SMC AVSS | 46 47 50 97 |
| | | THERMAL | SMC CPU 1V5 ISENSE | 46 50 |
| | | THERMAL | SMC CPU 1V5 ISENSE R | 50 |
| | | THERMAL | SMC CPU 1V5 VSENSE | 46 50 |
| | | THERMAL | GND SMC AVSS | 46 47 50 97 |
| | | THERMAL | SMC DIMM ISENSE | 46 50 |
| | | THERMAL | SMC DIMM 1V5 F | 50 |
| | | THERMAL | SMC DIMM VSENSE | 46 50 |
| | | THERMAL | GND SMC AVSS | 46 47 50 97 |
| | | THERMAL | SMC VCCSA ISENSE | 46 50 |
| | | THERMAL | SMC VCCSA ISENSE R | 50 |
| | | THERMAL | SMC VCCSA VSENSE | 46 50 |
| | | THERMAL | GND SMC AVSS | 46 47 50 97 |
| | | THERMAL | SMC PCH 1V05 ISENSE | 46 50 |
| | | THERMAL | SMC VAXG VSENSE | 46 50 |
| | | THERMAL | SMC PCH 1V05 VSENSE | 46 50 |
| | | THERMAL | GND SMC AVSS | 46 47 50 97 |
| | | THERMAL | SMC 1V05 ISENSE | 46 50 |
| | | THERMAL | SMC VAXG ISENSE | 46 50 |
| | | THERMAL | SMC 1V05 VSENSE | 46 50 |
| | | THERMAL | SMC GPU ISENSE | 46 50 |
| | | THERMAL | SMC GPU VSENSE | 46 50 |
| | | | | |
| | | THERMAL | SMC VCORE ISENSE | 46 50 |
| | | THERMAL | SMC VCORE VSENSE | 46 50 |
| | | | | |
| | | THERMAL | SMC CPU VSENSE | |

| | | | |
|--|----------------|----------------------|------|
| SYNC MASTER=K62 JERRY | | SYNC DATE=01/09/2011 | |
| PAGE TITLE | | | |
| SMC Constraints | | | |
|  Apple Inc. | DRAWING NUMBER | | SIZE |
| | 051-8442 | | D |
| | REVISION | | |
| | | 10.1.0 | |
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T29 ELECTRICAL ROUTES

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| T29_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| T29 | * | =5X_DIELECTRIC | ? | T29 | TOP,BOTTOM | =7X_DIELECTRIC | ? |

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| T29_SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| T29_SPI | * | 0.2 MM | ? |

T29 XTAL CONSTRAINTS

[illegible]

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| T29_XTAL | * | =4X_DIELECTRIC | ? |

T29 SMBUS INTERFACE CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| T29_SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| T29_SMB | * | =2x_DIELECTRIC | ? |

GREEN CLOCK CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_25M_5S5 | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_25M | * | =5X_DIELECTRIC | ? |

T29 BIAS CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| T29_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| T29_COMP | * | 0.2 MM | ? |

T29 NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | | |
|---------------------------|--------------|-------------|---------|-------------------------|-------------|
| | | PHYSICAL | SPACING | | |
| NO_TEST=TRUE | T29_90d | T29 | | T29 R2D C P<3..0> | 85 87 89 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 R2D C N<3..0> | 85 87 89 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 D2R C P<3..0> | 85 86 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 D2R C N<3..0> | 85 86 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 R2D P<3..0> | 85 87 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 R2D N<3..0> | 85 87 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 D2R P<3..0> | 85 87 89 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 D2R N<3..0> | 85 87 89 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 R2D C F P<3..0> | 85 87 |
| NO_TEST=TRUE | T29_90d | T29 | | T29 R2D C F N<3..0> | 85 87 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA ML P<3..0> | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA ML N<3..0> | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB ML P<3..0> | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB ML N<3..0> | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | DP A EXT AUXCH P | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | DP A EXT AUXCH N | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | DP SDRVA AUXCH C P | 85 |
| NO_TEST=TRUE | T29_90d | T29 | | DP SDRVB AUXCH C N | 85 |
| NO_TEST=TRUE | T29_90d | T29 | | DP SDRVA AUXCH C N | 87 |
| NO_TEST=TRUE | T29_90d | T29 | | DP B EXT AUXCH P | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | DP B EXT AUXCH N | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA D2R1 AUXCH P | 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA D2R1 AUXCH N | 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB D2R3 AUXCH P | 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB D2R3 AUXCH N | 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA ML C N<0> | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA ML C P<0> | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA ML C N<2> | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPA ML C P<2> | 85 86 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB ML C N<0> | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB ML C P<0> | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB ML C N<2> | 87 88 |
| NO_TEST=TRUE | T29_90d | T29 | | T29DPB ML C P<2> | 87 88 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 R2D P<3..0> | 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 R2D N<3..0> | 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 R2D C P<3..0> | 18 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 R2D C N<3..0> | 18 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 D2R P<3..0> | 18 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 D2R N<3..0> | 18 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 D2R C P<3..0> | 18 89 |
| NO_TEST=TRUE | PCIE_85d | PCIE | | PCIE T29 D2R C N<3..0> | 18 89 |
| NO_TEST=TRUE | CLK_PCIE_90d | CLK_PCIE | | PCIE CLK100M T29 P | 18 89 |
| NO_TEST=TRUE | CLK_PCIE_90d | CLK_PCIE | | PCIE CLK100M T29 N | 18 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC ML C P<3..0> | 84 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC ML C N<3..0> | 84 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC ML P<3..0> | 84 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC ML N<3..0> | 84 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 ML P<3..0> | 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 ML N<3..0> | 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 AUXCH P | 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 AUXCH N | 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 ML C P<3..0> | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 ML C N<3..0> | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 AUXCH C P | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK0 AUXCH C N | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK1 ML P<3..0> | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK1 ML N<3..0> | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK1 ML C P<3..0> | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK1 ML C N<3..0> | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK1 AUXCH C P | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SNK1 AUXCH C N | 79 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC AUXCH R C P | 84 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC AUXCH R C N | 84 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC AUXCH C P | 84 89 |
| NO_TEST=TRUE | DP_85d | DISPLAYPORT | | DP T29SRC AUXCH C N | 84 89 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA AUXCH P | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA AUXCH N | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB AUXCH P | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB AUXCH N | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA ML C P<3..0> | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA ML C N<3..0> | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA ML P<3..0> | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA ML N<3..0> | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA ML R P<3..0> | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVA ML R N<3..0> | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB ML C P<3..0> | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB ML C N<3..0> | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB ML P<3..0> | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB ML R P<3..0> | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | DP SDRVB ML R N<3..0> | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | T29 A RSPD N | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | T29 A RSPD P | 85 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | T29 B RSPD N | 87 |
| NO_TEST=TRUE | T29_90d | DISPLAYPORT | | T29 B RSPD P | 87 |

T29 NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | | NET_TYPE | | | |
|---------------------------|---------------|----------|-----------------------|----|----------|
| | PHYSICAL | SPACING | | | |
| | T29_SPT_55G | T29_SPT | JTAG T29 TDI | 15 | 21 89 |
| | T29_SPT_55G | T29_SPT | JTAG T29 TMS | 15 | 18 89 |
| | T29_SPT_55G | T29_SPT | JTAG T29 TCK | 15 | 21 25 |
| | T29_SPT_55G | T29_SPT | JTAG T29 TDO | 15 | 21 89 |
| RE30 | T29_SPT_55G | T29_SPT | T29 SPI MOSI | | 89 |
| RE30 | T29_SPT_55G | T29_SPT | T29 SPI MISO | | 89 |
| RE30 | T29_SPT_55G | T29_SPT | T29 SPI CS L | | 89 |
| RE30 | T29_SPT_55G | T29_SPT | T29 SPI CLK | | 89 |
| | CLK_25M_55G | CLK_25M | SYSCLK CLK25M T29 | 80 | 89 99 |
| | CLK_25M_55G | CLK_25M | SYSCLK CLK25M T29 R | 89 | 99 |
| | T29_SMB_55G | T29_SMB | I2C T29 SDA | 49 | 89 |
| | T29_SMB_55G | T29_SMB | I2C T29 SCL | 49 | 89 |
| RE30 | CLK_25M_55G | CLK_25M | SYSCLK CLK25M SB | | 80 |
| RE30 | CLK_25M_55G | CLK_25M | SYSCLK CLK25M ENET | | 80 |
| RE30 | CLK_25M_55G | CLK_25M | ENET CLK25M XTALI OSC | 36 | 80 |
| RE30 | CLK_25M_55G | CLK_25M | SYSCLK CLK25M T29 CLK | | 80 |
| RE30 | CLK_25M_55G | CLK_25M | SYSCLK CLK25M T29 | | 80 89 99 |
| RE30 | CLK_25M_55G | CLK_25M | SYSCLK CLK25M T29 R | 89 | 99 |
| RE30 | T29_XTAL_100D | T29_XTAL | SYSCLK CLK25M X2 | | 89 |
| RE30 | T29_XTAL_100D | T29_XTAL | SYSCLK CLK25M X2 R | | 89 |
| RE30 | T29_XTAL_100D | T29_XTAL | SYSCLK CLK25M X1 | | 89 |
| RE30 | T29_55G | T29_COMP | T29 RSENSE | | 89 |
| RE30 | T29_55G | T29_COMP | T29 RBIAS | | 89 |
| RE30 | | T29_COMP | T29 A BIAS | 79 | 83 85 88 |
| RE30 | | T29_COMP | T29 B BIAS | 79 | 83 87 88 |
| RE30 | | T29_COMP | DP A BIAS | 79 | 85 |


PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| PM | * | * | 2:1_SPACING |
| PM_VTT | PM_VTT | * | 2:1_SPACING |
| PM_VTT | * | * | 3:1_SPACING |
| PM_VTT | GND | * | DEFAULT |
| PM | GND | * | DEFAULT |

| NET_TYPE | | | |
|----------|---------|-----------------------|-----------|
| PHYSICAL | SPACING | | |
| PM | | 4V5 REG EN | 56 |
| PM | | 3V42Q3H SHDN L | 73 |
| PM | | ALL SYS PWRGD R | 5 32 64 |
| PM | | ALL SYS PWRGD SMC | 46 64 |
| PM | | AP PWR EN | 20 25 33 |
| PM | | AP MINI RESET L | 33 |
| PM | | AUD I2C INT L | 20 62 |
| PM | | AUD IP PERIPHERAL DET | 20 61 |
| PM | | AUD IPHS SWITCH EN | 21 62 |
| PM | | AUD SPDIF IN | 60 84 94 |
| PM | | AUD SPDIF IN CODEC | 56 84 |
| PM | | BDV_BKL_PWM | 46 84 100 |
| PM | | BL_PWM | 6 84 |
| PM | | BL_EN | 6 82 |
| PM | | BDV_BKL_PWM | 46 84 100 |
| PM | | CK505 27MHZ EN | 26 |
| PM | | CPUVTT REG EN | |
| PM_VTT | | CPUVTT REG PGOOD R | 63 |
| PM | | CPU MEM RESET L | 11 32 |
| PM | | CPU Peci R | 46 |
| PM_VTT | | CPU PWRGD | 11 21 25 |
| PM | | CPU RESET L | 11 27 |
| PM | | CPU SKTOCC L | 11 63 |
| PM | | CPU CATERR L | 11 |
| PM | | CPU Peci | 11 21 46 |
| PM | | CPU PROCHOT L | 11 47 65 |
| PM | | CPU THRMTrip L | 11 47 |
| PM | | CPU PROC_SEL | 11 19 |
| PM | | DEBUG RESET L | 27 48 |
| PM | | DDRVT EN | |
| PM | | DP INT SPDIF AUDIO | 82 84 |
| PM | | DP INTFNL HPD | 82 84 |
| PM | | 3V3R2V9 DPAPWR ADJ | 83 98 |
| PM | | DP A PWRDWN | 83 |
| PM | | DP A PWRDWN FET R | 83 |
| PM | | DP A PWRDWN INV | 83 |
| PM | | DPAPWRSW HVEN L R | 83 |
| PM | | DPAPWRSW CT | 83 |
| PM | | DPAPWRSW_ILIM | 83 |
| PM | | DPAPWRSW_ILIT | 83 |
| PM | | T29 A HV EN | 83 85 |
| PM | | 3V3R2V9 DPBPWR ADJ | 83 |
| PM | | DP B PWRDWN | 83 |
| PM | | DP B PWRDWN FET R | 83 |
| PM | | DP B PWRDWN INV | 83 |
| PM | | DPBPWRSW HVEN L R | 83 |
| PM | | DPBPWRSW CT | 83 |
| PM | | DPBPWRSW_ILIM | 83 |
| PM | | DPBPWRSW_ILIT | 83 |
| PM | | T29 B HV EN | 83 87 |
| PM | | T29 PWR EN | 18 81 100 |
| PM | | T29 RESET RTR L | 81 89 |
| PM | | LCD_BL_FILT | 84 |
| PM | | LCD_BLK_ON_DLY | 84 |
| PM | | LCD_BL_PWM | 84 |
| PM | | MXM_PNL_BL_PWM | 77 84 |

| NET_TYPE | | | |
|----------|---------|---------------------------|--------------|
| PHYSICAL | SPACING | | |
| PM | | ENET PWR EN | 20 25 36 |
| PM | | ENET LOW PWR | 15 21 37 |
| PM | | FW RESET L | 27 39 |
| PM | | ENET RESET L | 27 36 |
| PM | | FW PME L | 15 21 39 |
| PM | | FW PWR EN | 15 21 |
| PM | | FW CLKREQ L | 15 39 |
| PM | | ISOLATE CPU MEM L | 21 25 32 |
| PM | | LPC PWRDWN L | 19 46 48 |
| PM | | MEM RESET L | 30 31 32 92 |
| PM | | MINI_CLKREQ L | 15 33 |
| PM | | MINI_RESET L | 27 33 |
| PM | | MXM_CLKREQ L | 9 76 |
| PM | | MXM_GOOD | 5 21 25 |
| PM | | ODD PWR EN L | 15 21 42 |
| PM | | RTC RESET L | 18 27 100 |
| PM | | RSRST PWRGD | 46 64 |
| PM | | RTC RESET L | 18 27 100 |
| PM | | S4_ENABLES | 63 |
| PM | | SDCONN_STATE_RST_L | |
| PM | | SDCONN_DETECT_BUF_L | 95 |
| PM | | SDCONN_STATE_CHANGE | 20 26 46 |
| PM | | SDCARD RESET | 15 21 44 101 |
| PM | | SDCARD RESET L | 44 |
| PM | | SDCARD_PLT_RST_L | 27 44 |
| PM | | SDCARD_PLT_RST_L_R | |
| PM | | SMC PM G2 EN | 46 75 |
| PM | | SMC PM G2 EN R | 75 |
| PM | | SMC PM G2 EN L | 75 |
| PM | | S5 DG 1 | 75 |
| PM | | S5 MSFT G1 | 75 |
| PM | | USE HDD OOB L | 20 51 |
| PM | | HDD OOB 1V00 REF | 51 |
| PM | | SMC ADAPTER EN | 19 46 47 |
| PM | | SMC RUNTIME SCI L | 21 46 47 |
| PM | | SMC WAKE SCI L | 15 18 21 46 |
| PM | | SMC DELAYED PWRGD | 47 64 |
| PM | | SMC LRESET L | 27 46 |
| PM | | SMC RESET L | 46 47 48 |
| PM | | SMC PROCHOT | 46 47 |
| PM | | SMC PROCHOT 3 3 L | 46 47 |
| PM | | SMC ONOFF L | 46 47 |
| PM | | SMC MANUAL_RST_L | 47 |
| PM | | SPI_DESCRIPTOR_OVERRIDE_L | 18 46 |
| PM | | T29 PWR EN | 18 81 100 |
| PM | | T29 RESET L | 27 81 |
| PM | | T29 DP PORTA PWR EN | 20 25 83 94 |
| PM | | T29 DP PORTA PWR EN REG | 83 |
| PM_VTT | | XDP_CPUPWRGD | |
| PM_VTT | | XDP_DBRESET L | 11 25 |
| PM_VTT | | XDP_PWRGD | |
| PM | | XDPPCH_PLTRST L | 25 27 |
| PM | | USB_HUB_SOFT_RESET_L | 20 25 34 |
| PM | | VSYNC_DP_CONN | 6 82 |
| PM | | VSYNC_DP | 82 |
| PM | | VIDEO_ON | 62 |
| PM | | VTT_REG_PGOOD_L | 63 |

| NET_TYPE | | | |
|----------|---------|------------------------|------------------------|
| PHYSICAL | SPACING | | |
| PM | | PLT RESET L | 20 27 |
| PM_VTT | | PLT RESET LS1V05 L | 11 |
| PM | | PM BATLOW L | 15 19 46 |
| PM | | PM CLK32K_SUSCLK | 9 46 94 |
| PM | | PM CLK32K_SUSCLK_R | 9 19 94 |
| PM | | PM CLKRUN L | 15 19 46 48 |
| PM | | PM PWRBTN L | 19 25 46 |
| PM | | PM RSMRST L | 27 46 |
| PM | | PM RSMRST_PCH_L | 19 27 |
| PM | | PCH_SRTCST L | 18 |
| PM | | PCH_INTVRMEN L | 18 |
| PM | | PCH_DSMVRMEN | 19 |
| PM | | PCH_DF_TVS | 19 |
| PM | | PCH_PROCPWRGD | 21 |
| PM | | PCIE_WAKE_L | 19 33 36 79 |
| PM | | PM_DSW_PWRGD | 19 |
| PM | | PM_ASW_PWRGD | 19 64 |
| PM | | PM_MEM_PWRGD_R | 11 |
| PM | | PM_EN_DDR1V5_S3_REG | 63 72 |
| PM | | PM_EN_DDRVTT_S0_REG | 32 63 72 |
| PM | | PM_EN_P12V_S0_FET | 6 63 |
| PM | | PM_EN_P1V05_S0_REG | 63 68 |
| PM | | PM_EN_P1V05_S3_REG | |
| PM | | PM_EN_P1V5_S0_FET | 63 74 |
| PM | | PM_EN_P1V8_S0_REG | 63 72 |
| PM | | PM_EN_P3V3_S0_FET | 63 74 |
| PM | | PM_EN_P3V3_S3_FET | 63 74 |
| PM | | PM_EN_P3V3_S5_REG | 71 |
| PM | | PM_EN_P5V_S0_FET | 63 74 |
| PM | | PM_EN_P5V_S3_REG | 63 71 |
| PM | | PM_EN_PVCCSA_S0_REG_L | 64 |
| PM | | PM_EN_VCCSA_S0_CPU | |
| PM | | PM_EN_PVCORE_CPU | 63 65 |
| PM_VTT | | PM_MEM_PWRGD | 11 19 100 |
| PM | | PM_MXM_EN | 64 77 |
| PM | | PM_PCH_PWRGD_R | 64 |
| PM | | PM_PECI_PWRGD | 46 64 |
| PM | | PM_PECI_PWRGD_R | 46 |
| PM | | PM_PGOOD_DDR1V5_S3_REG | 5 63 72 |
| PM | | PM_PGOOD_P1V05_S0_REG | 63 64 68 |
| PM | | PM_PGOOD_P1V5_S0_FET | 11 64 74 |
| PM | | PM_PGOOD_P1V8_S0_REG | 64 72 |
| PM | | PM_PGOOD_P3V3_S0_FET | 63 64 74 |
| PM | | PM_PGOOD_P3V3_S3_FET | 34 74 |
| PM | | PM_PGOOD_P3V3_S5_REG | 27 64 71 |
| PM | | PM_PGOOD_P5V_S0_FET | 63 64 74 |
| PM | | PM_PGOOD_MINI | 33 |
| PM | | PM_PGOOD_PVCORE_CPU | 5 25 64 65 |
| PM | | PM_PGOOD_PVCCSA_S0_REG | 63 64 |
| PM | | PM_PGOOD_P5V_S3_REG | 63 71 83 |
| PM | | PM_PGOOD_PVAXG | 5 65 |
| PM_VTT | | PM_MEM_PWRGD | 11 19 100 |
| PM | | PM_MEM_PWRGD_L | 11 |
| PM | | PM_MXM_PGOOD | 64 77 |
| PM | | PM_PCH_PWRGD | 19 21 64 |
| PM | | PM_SLP_S3_5V | 32 |
| PM | | PM_SLP_S3_5V_L | 32 |
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| PM | | PM_SLP_S3_L | 5 19 26 32 36 46 47 63 |
| PM | | PM_SLP_S4_L | 5 19 32 46 47 63 100 |
| PM | | PM_SLP_S5_L | 5 19 46 47 63 |
| PM_VTT | | PM_SYNC | 11 19 |
| PM | | PM_SYSRST_L | 19 25 27 46 |
| PM | | PM_SYS_PWRGD | 19 32 64 |
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| PM | | PM_SLP_S4_L | 5 19 32 46 47 63 100 |
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| PM | | PGOOD_PCH_S0_R | 64 94 |
| PM | | PGOOD_SYSPWR0K | 64 |
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